T13Fv SCHEMATIC R1.11

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56	POWER_VGA_RAM(Empty)
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59	POWER_DETECT
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<Variant Name>

ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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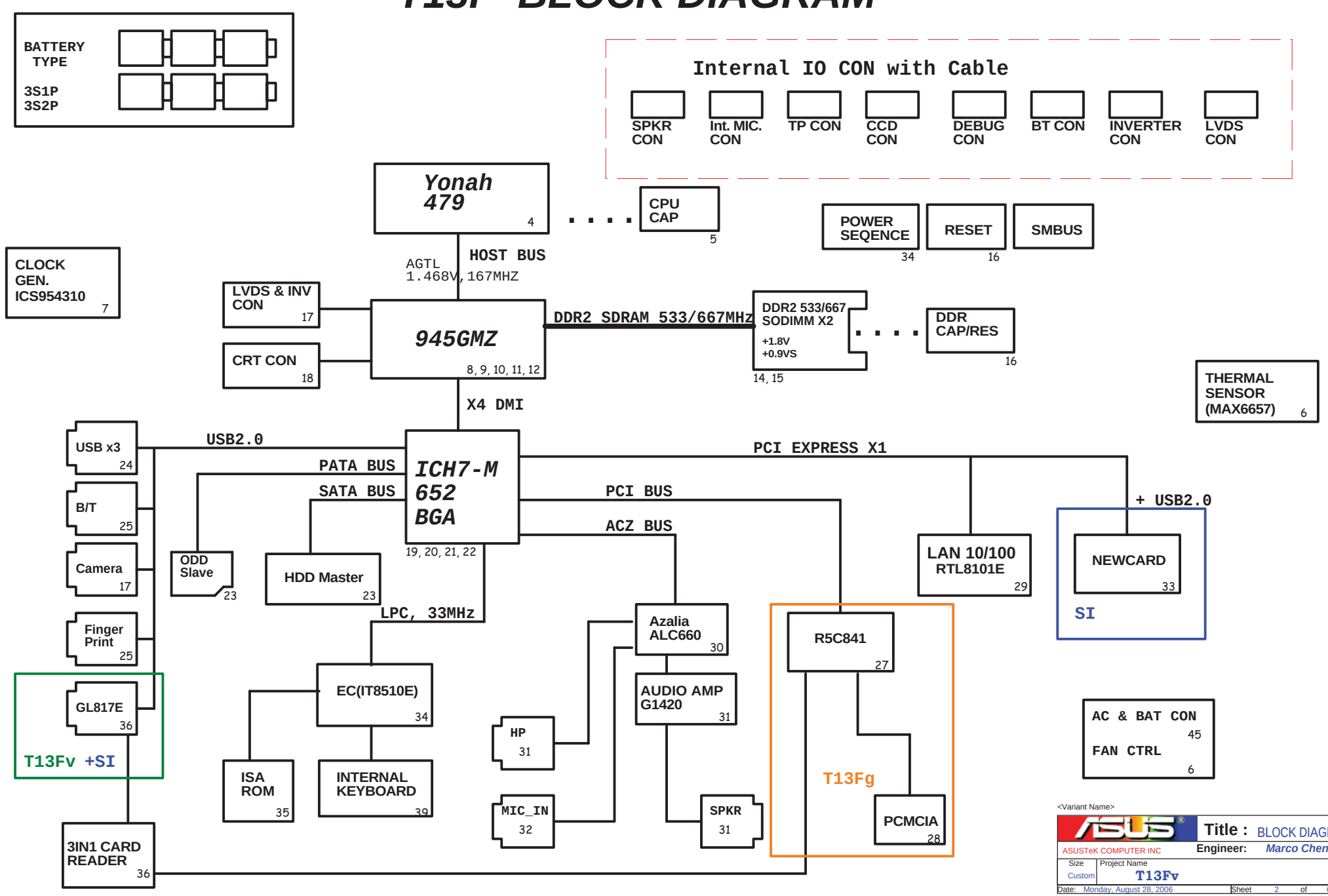
T13F BLOCK DIAGRAM



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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	CR_DRIVER#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	CR_POWER#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	PWRLMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

ICH7M_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

ICH7M_PCI_DEVICE:

PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

ICH7M_GPIO

Pin		Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BT_LED_EN	+3VS
GPIO 07	i	GPI	N/A	+3VS
GPIO 08	i	GPI	EXTSMI#	+3VSUS
GPIO 09	i	GPI	N/A	+3VSUS
GPIO 10	i	GPI	N/A	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KBC_SCI#	+3VSUS
GPIO 13	i	GPI	N/A	+3VSUS
GPIO 14	i	GPI	N/A	+3VSUS
GPIO 15	i	GPO	802_LED_EN	+3VSUS
GPIO 16	O	0 GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1 GPO	PCI_GNT#5	+3VS
GPIO 18	O	1 GPO	STP_PCI#	+3VS
GPIO 19	i	1 GPI	N/A	+3VS
GPIO 20	O	1 GPO	STP_CPU#	+3VS
GPIO 21	i	1 GPO	N/A	+3VS
GPIO 22	i	1 Native	PCI_REQ#4	+3VS
GPIO 23	i	1 Native	N/A	+3VS
GPIO 24	O	0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1 GPO	CB_SD#	+3VSUS
GPIO 26	O	0 GPO	BT_ON#	+3VSUS
GPIO 27	O	0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0 GPO	MEMROM/YONAH#	+3VSUS
GPIO 29	i	0 Native	USB_OC#5	+3VSUS
GPIO 30	i	0 Native	USB_OC#6	+3VSUS
GPIO 31	i	0 Native	USB_OC#7	+3VSUS
GPIO 32	O	1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1 GPO	N/A	+3VS
GPIO 34	O	0 GPO	CPU_Select	+3VS
GPIO 35	O	0 GPO	N/A	+3VS
GPIO 36	i	0 GPO	N/A	+3VS
GPIO 37	i	0 GPI	PCB_ID0	+3VS
GPIO 38	i	0 GPI	PCB_ID1	+3VS
GPIO 39	i	0 GPI	PCB_ID2	+3VS
GPIO [40:47]		NA	NA	NA
GPIO 48		Native	PCI_GNT#4	+3VS
GPIO 49		Native	H_PWRGD	+VCORE

<Variant Name>

Title : Schematic data

ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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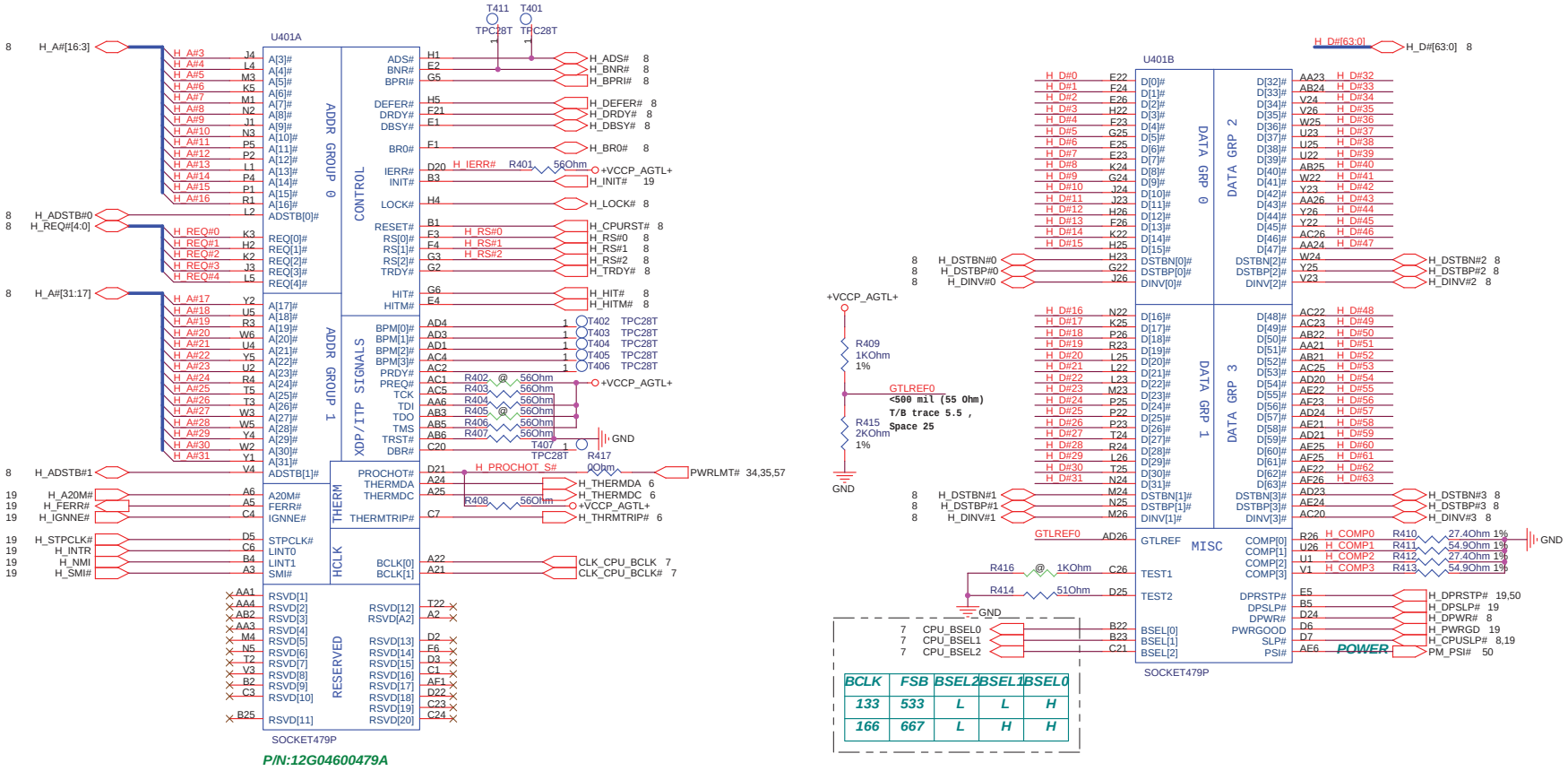

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<Variant Name>

Title : YONAH CPU (1)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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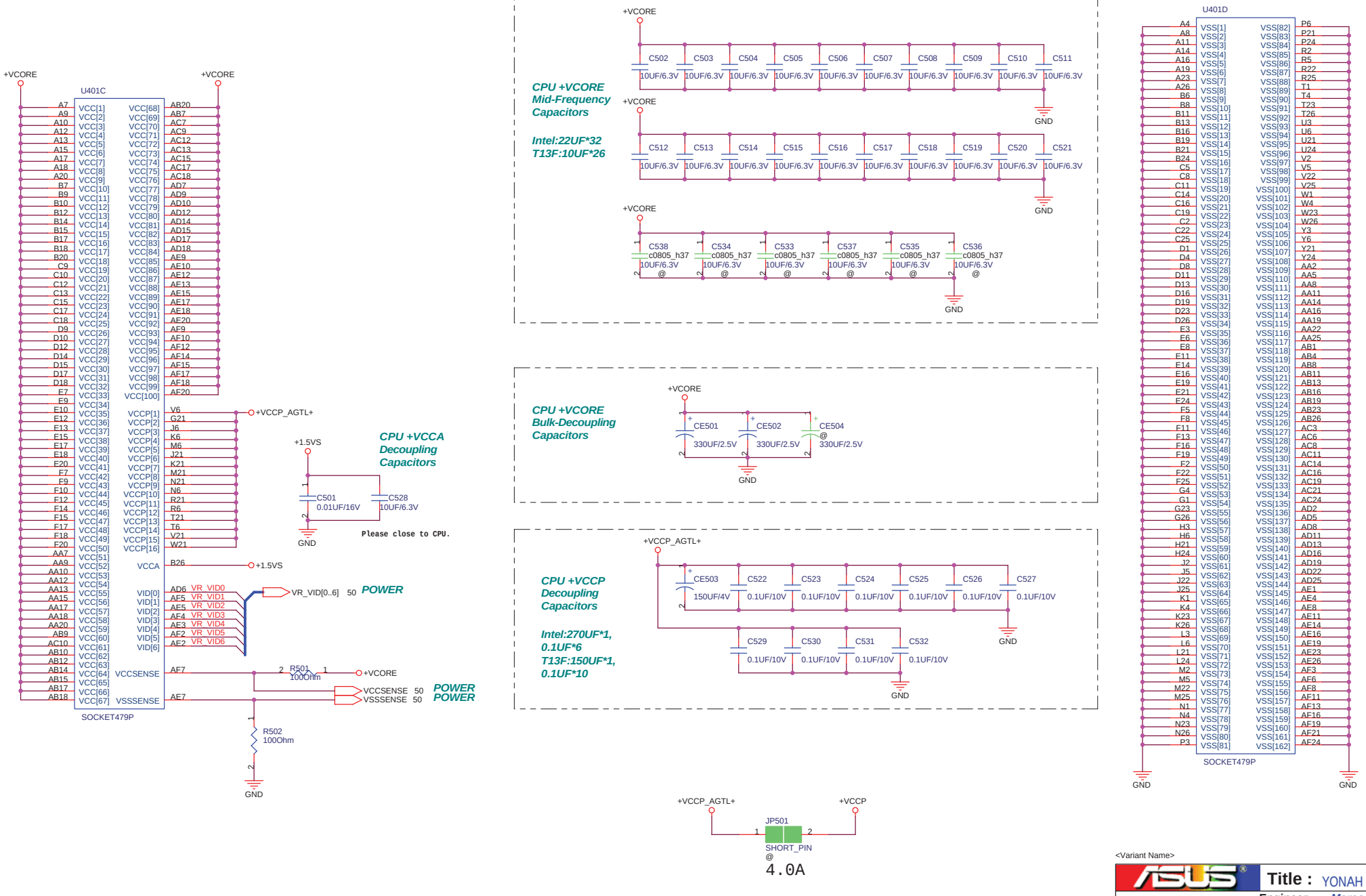

<Variant Name>

ASUSTeK COMPUTER INC	Title : YONAH CPU (2)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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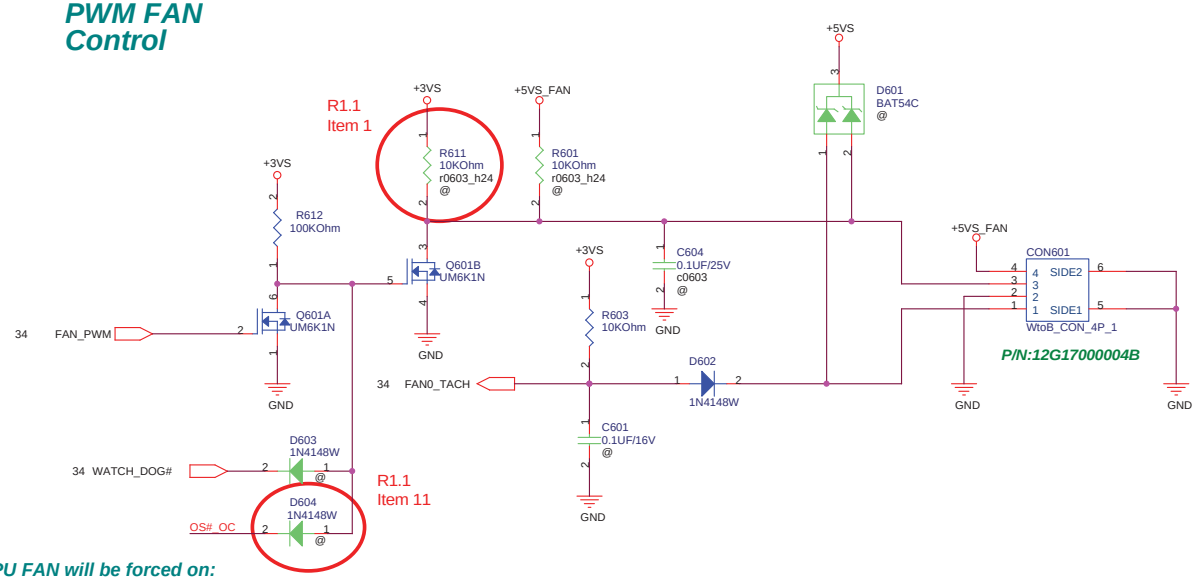
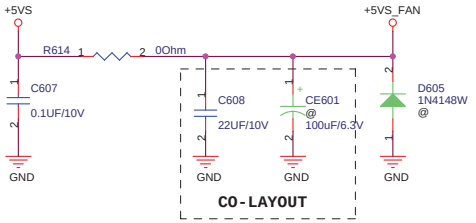
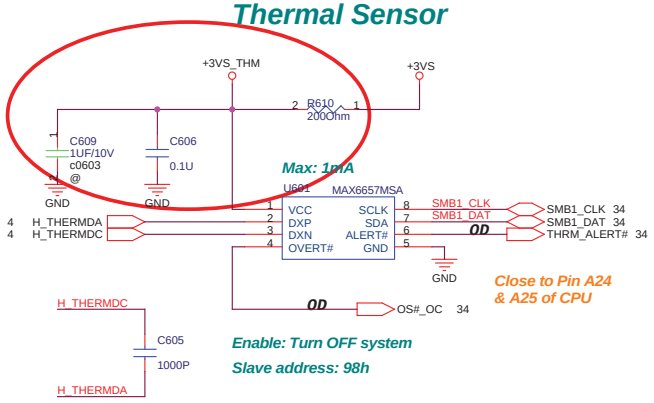
PWM FAN Control

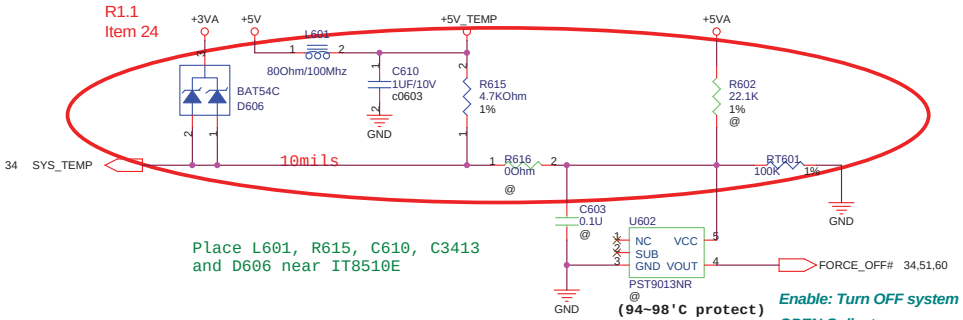


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

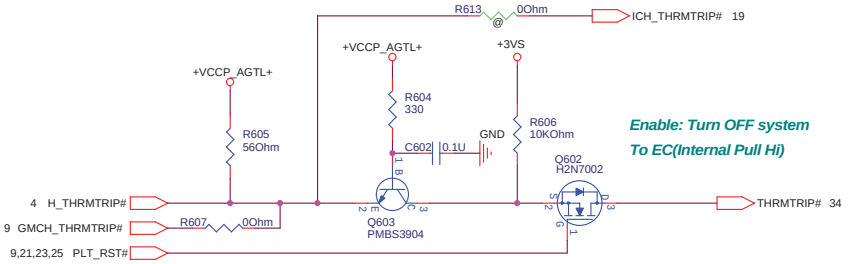


Thermal Sensor





Place L601, R615, C610, C3413
and D606 near IT8510E



<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thernal	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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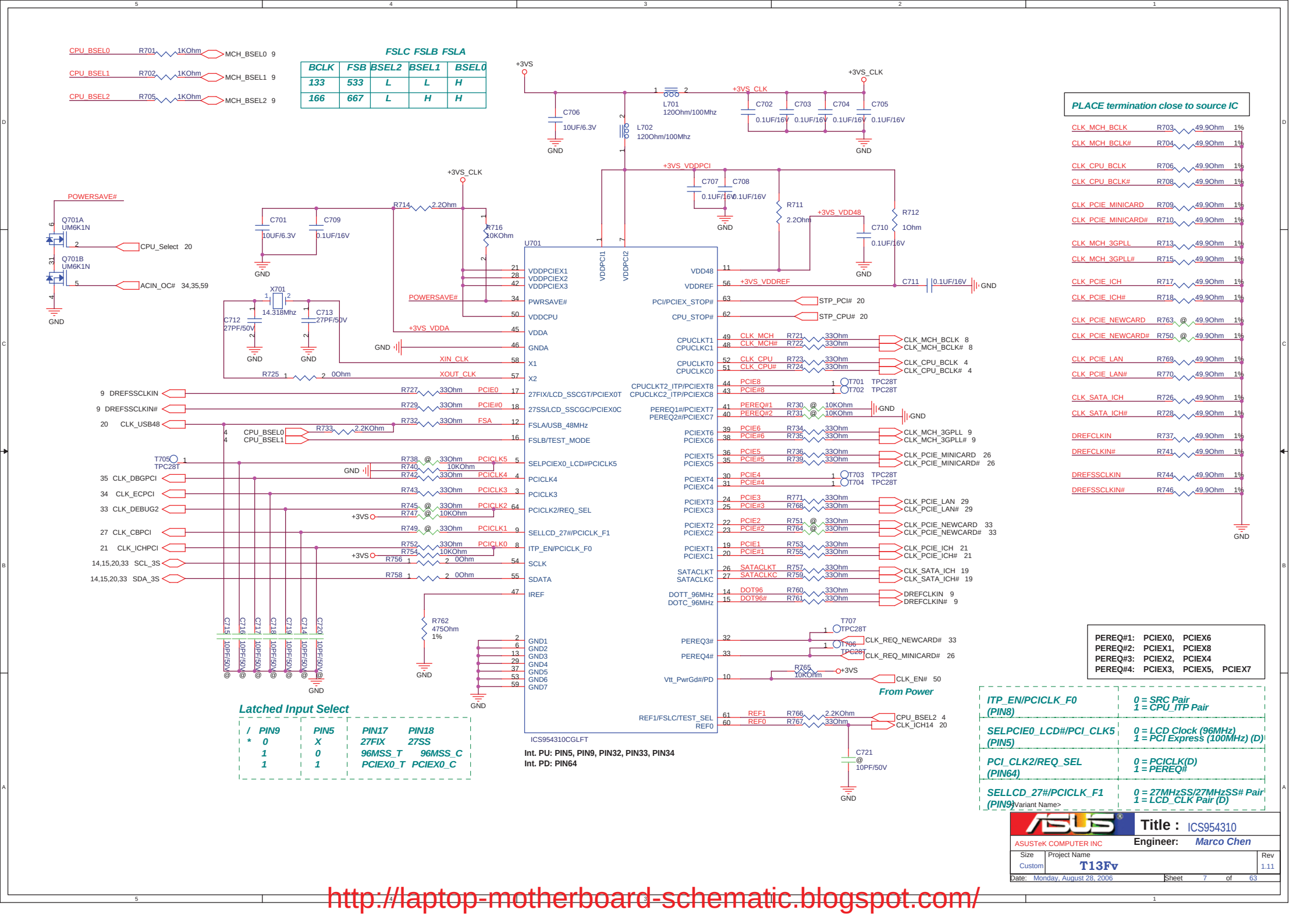

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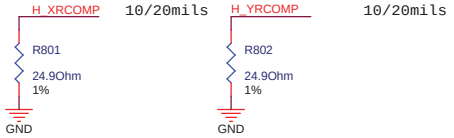
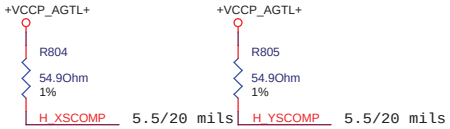
RCOMP

For Calibrating FSB I/O Buffer



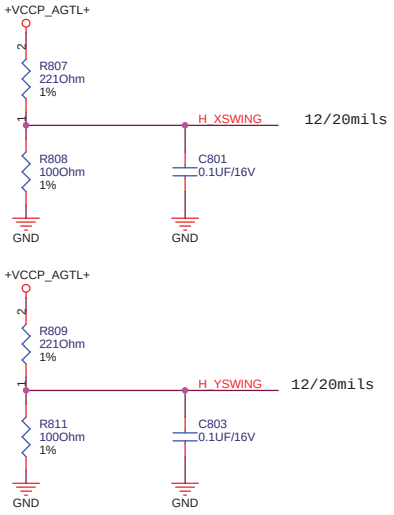
SCOMP

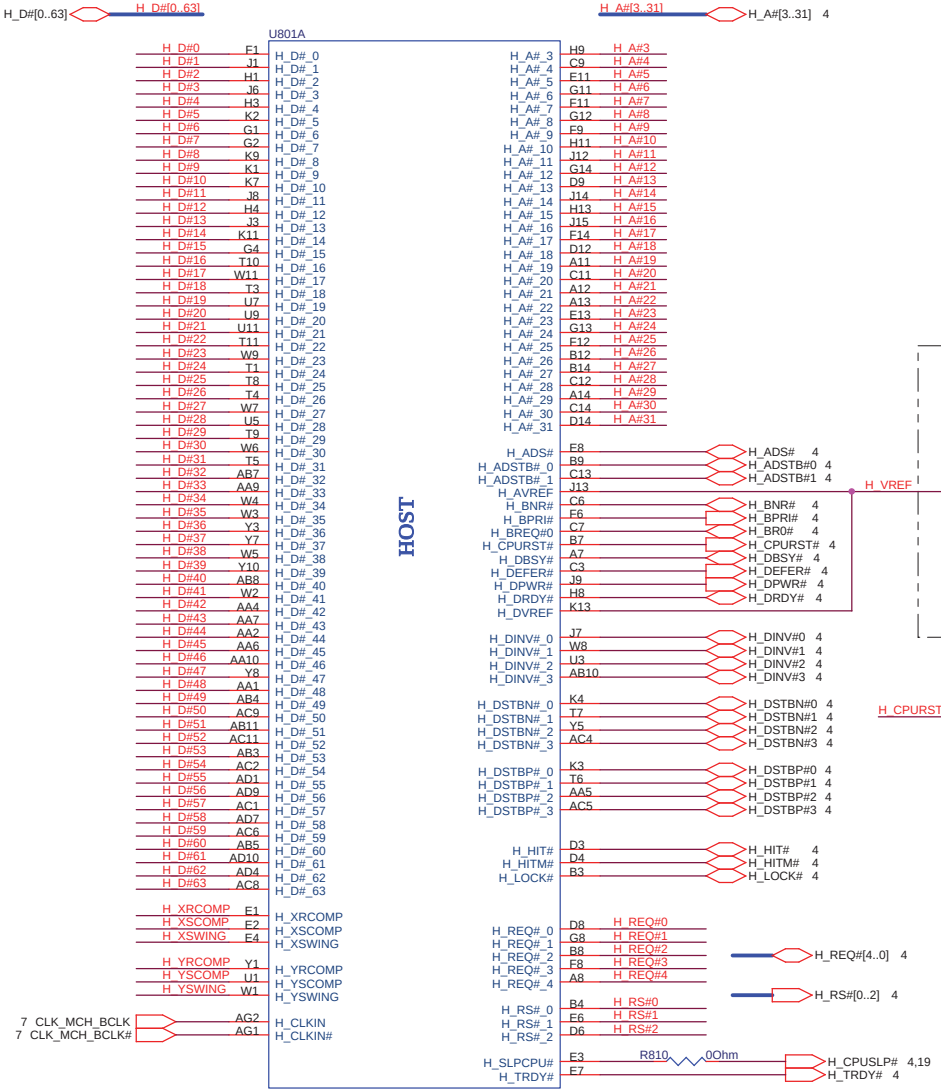
For Slew Rate Compensation on the FSB



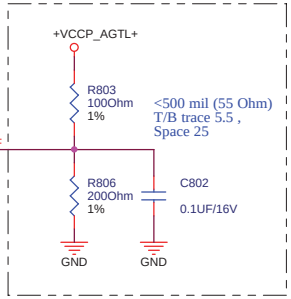
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit





AGTL+ I/O Voltage Reference



<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--CPU

Engineer: Marco Chen

Size	Project Name	Rev
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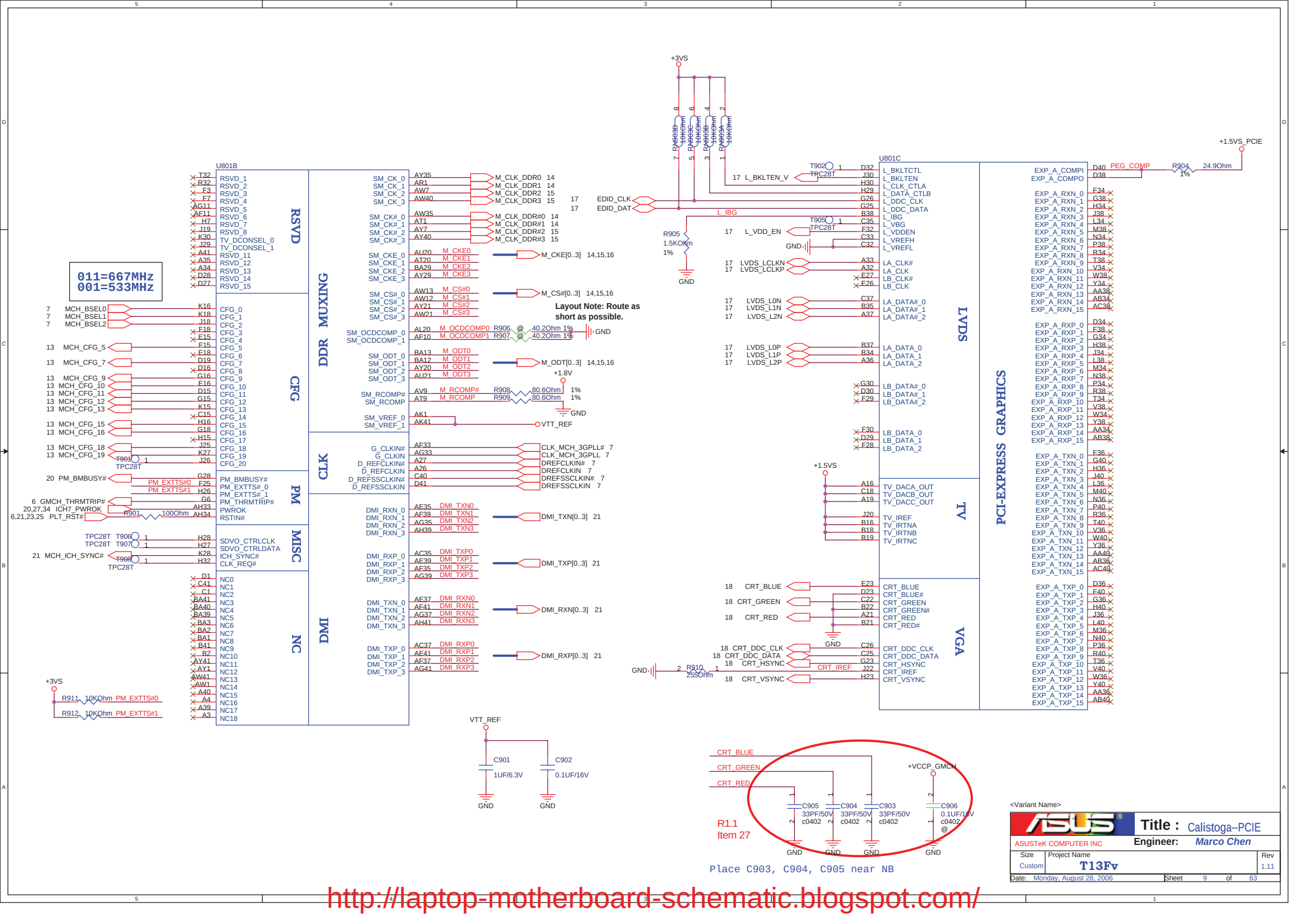

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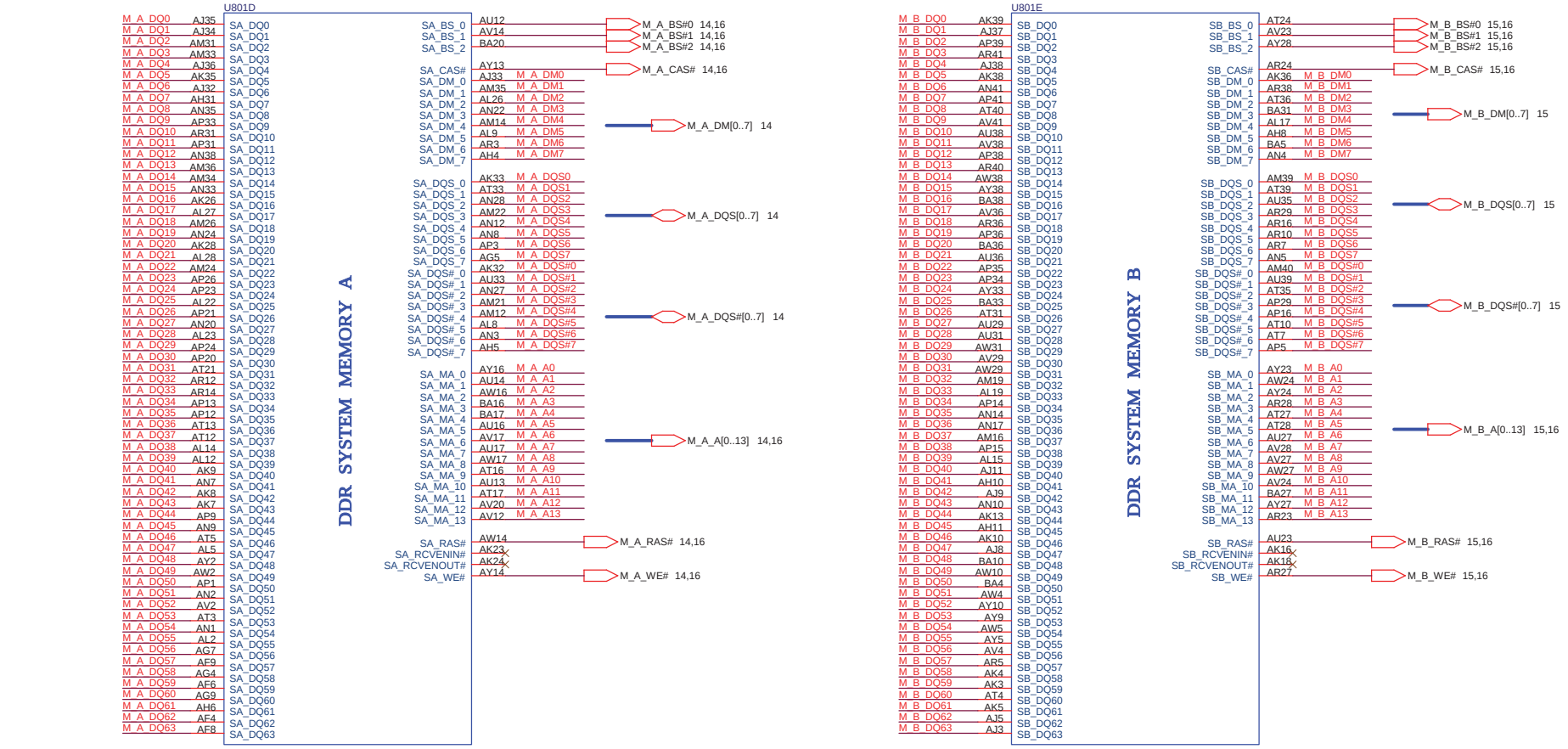
14 M_A_DQ[0..63]

15 M_B_DQ[0..63]



<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--DDR2

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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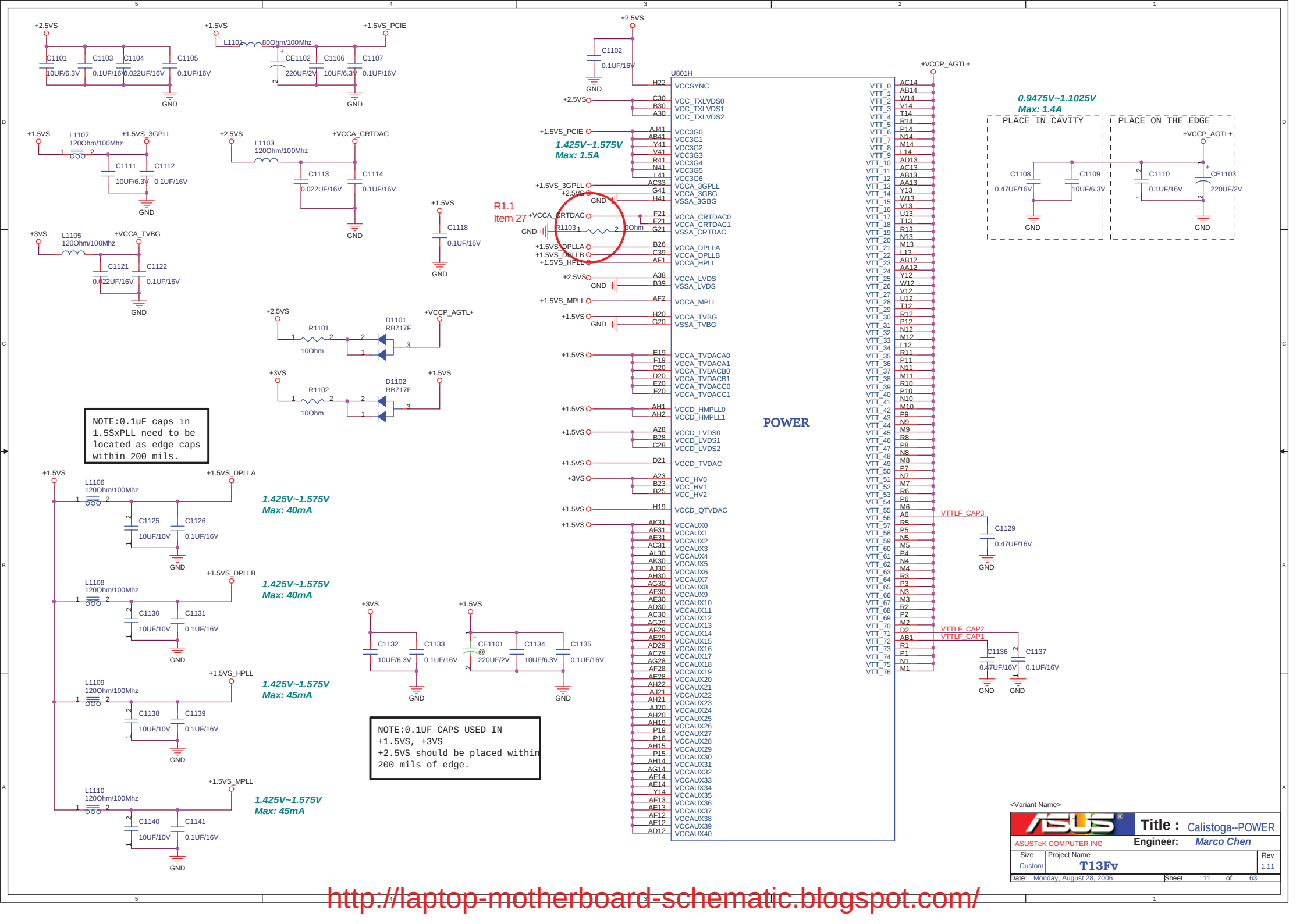

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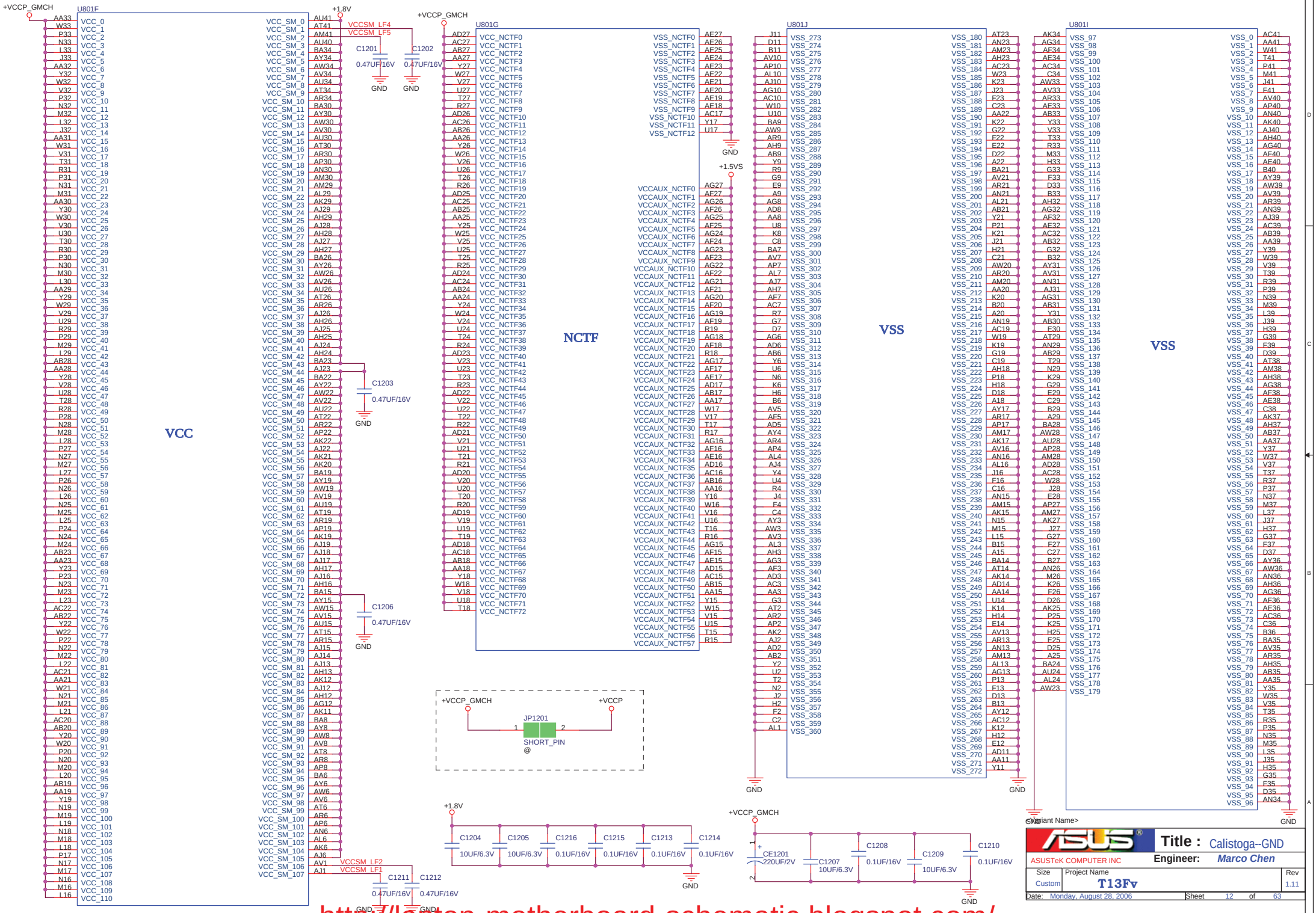

Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--GND

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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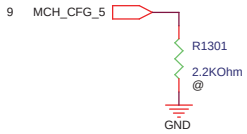
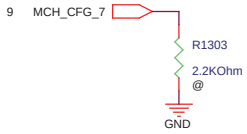


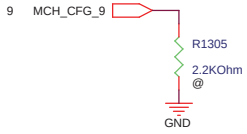
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



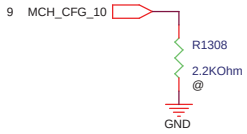
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



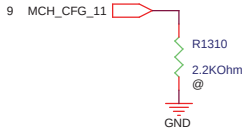
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

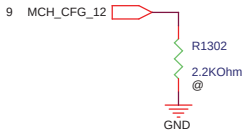
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

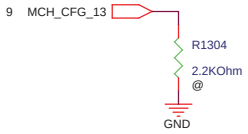
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

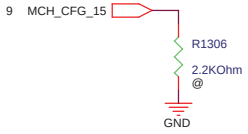
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG[13:12] : GMCH TEST MODE SELECT

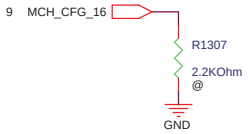
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)





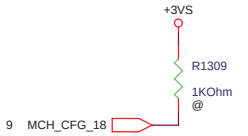
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V

CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga--Strap	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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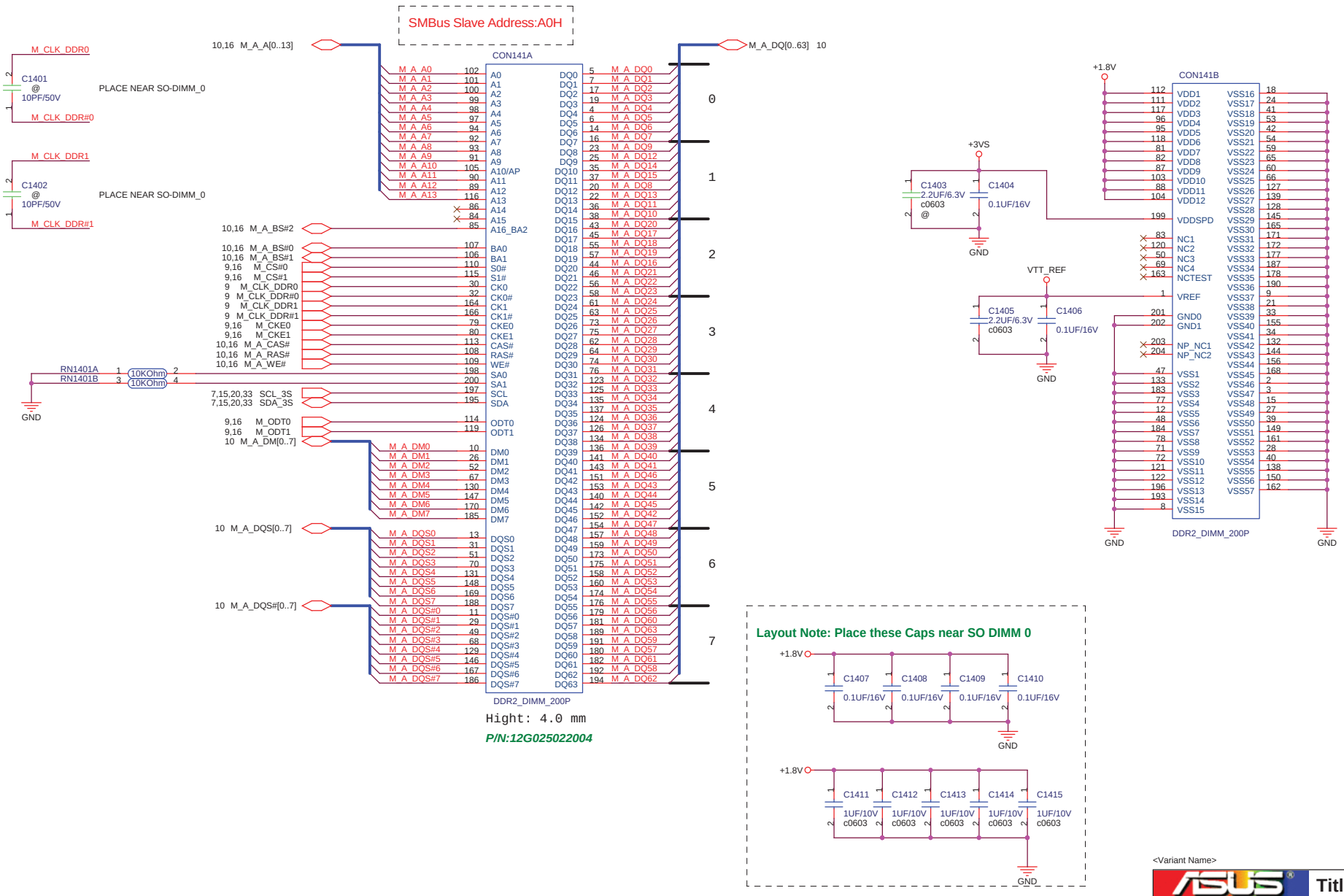
http://laptop-motherboard-schematic.blogspot.com/

DDR2 HAD SWAPED.

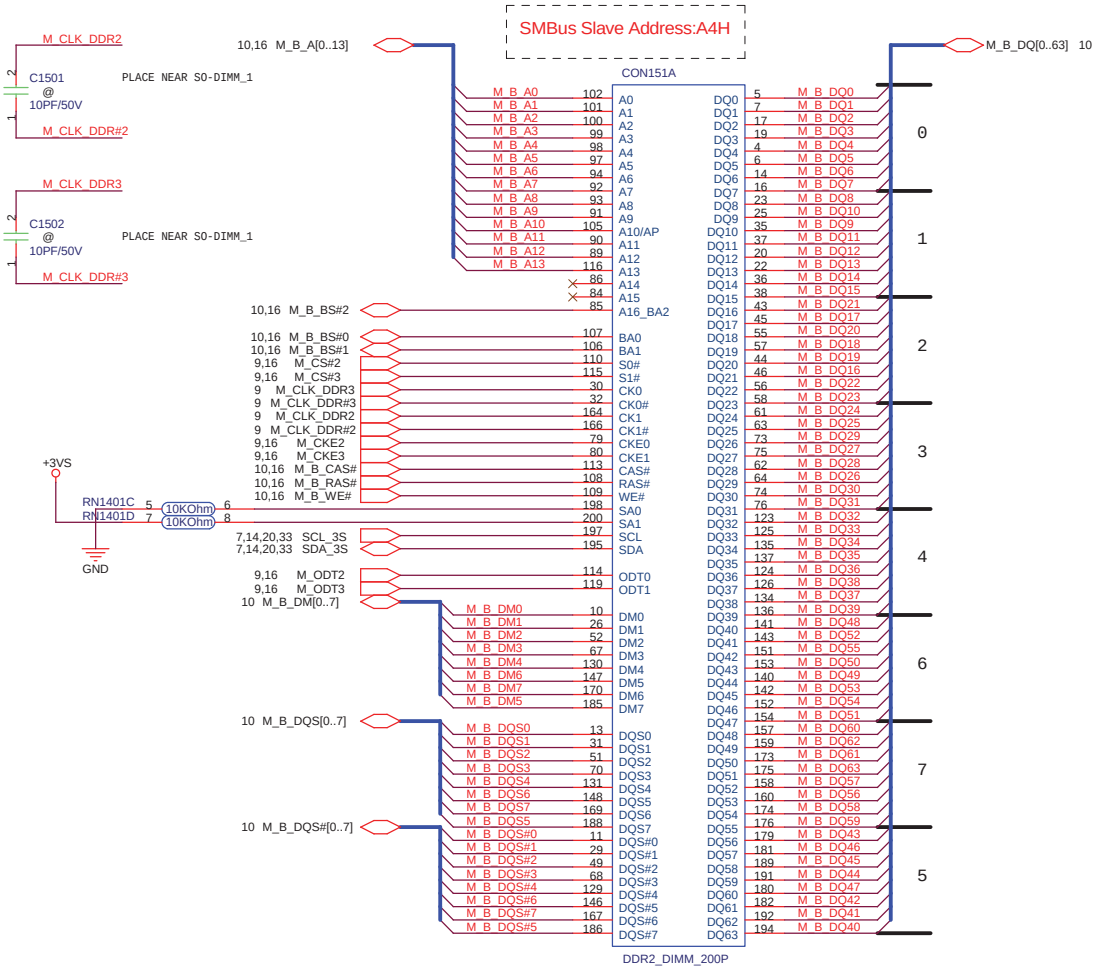


<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 14 of 63	

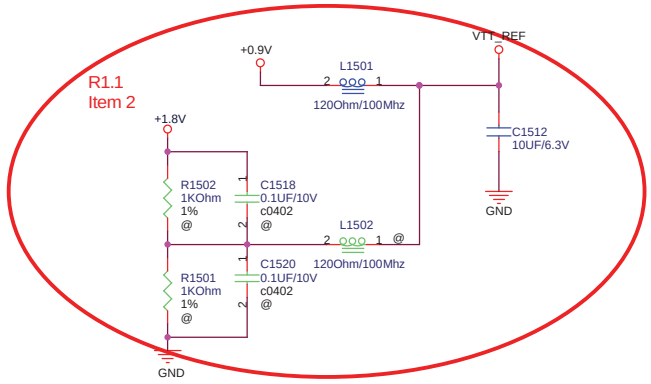
http://laptop-motherboard-schematic.blogspot.com/

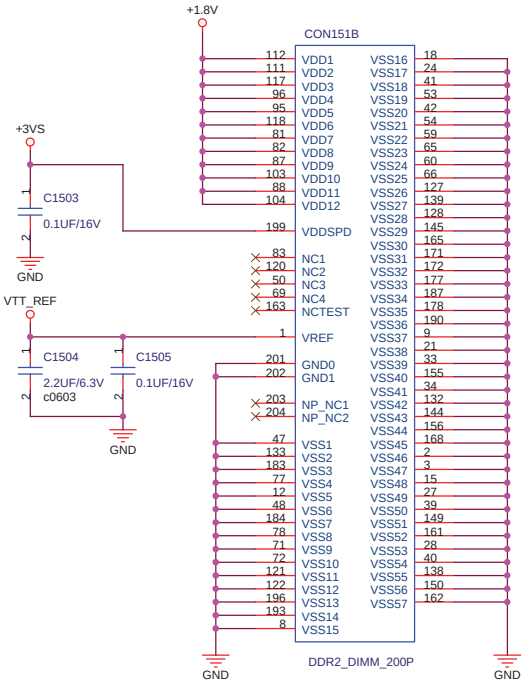
DDR2 HAD SWAPED.

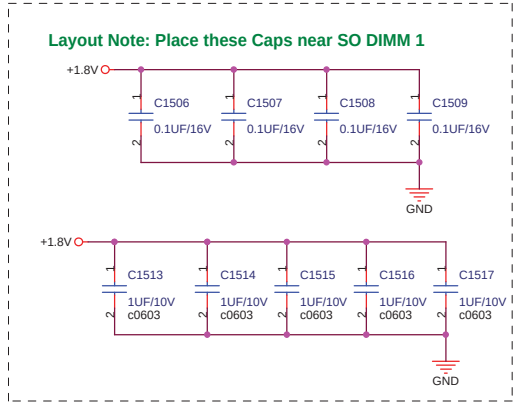


Hight: 9.2 mm

P/N:12G025C22004





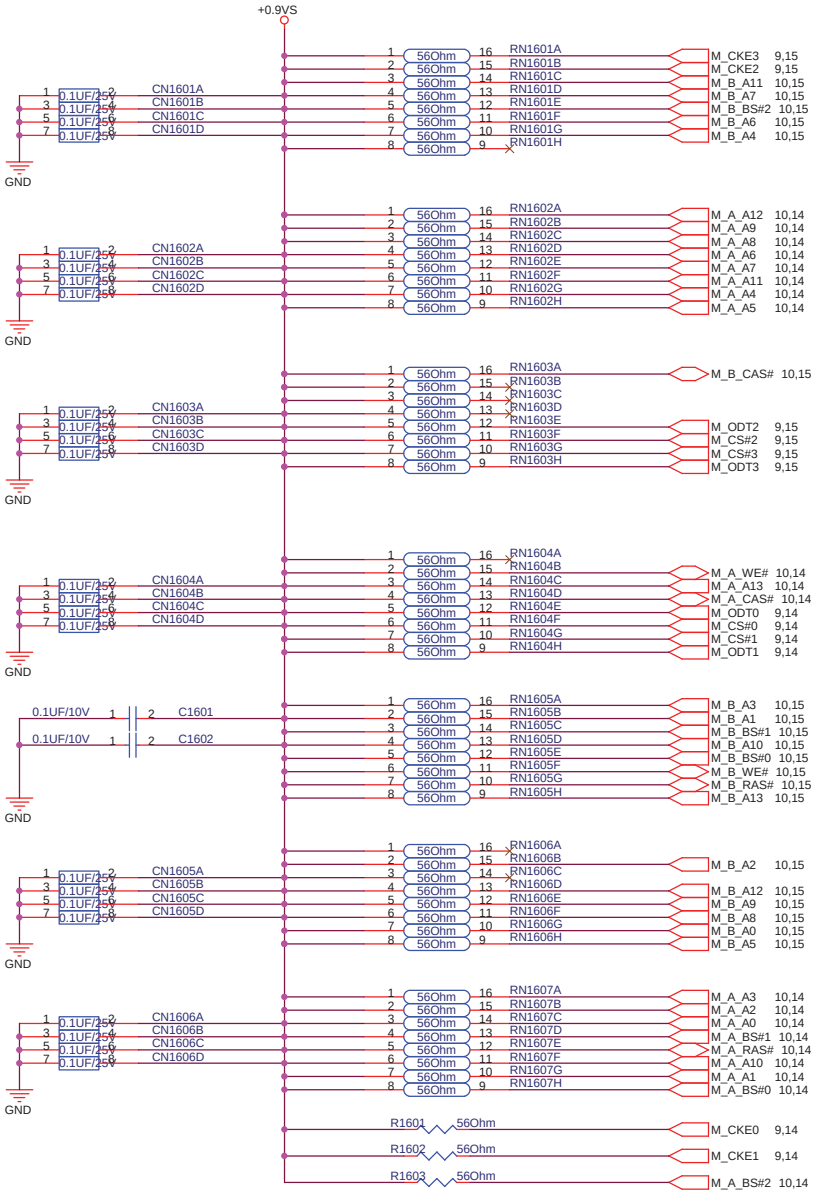


<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_1	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 15 of 63	

http://laptop-motherboard-schematic.blogspot.com/

DDR2 HAD SWAPED.



Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 TERMINATION

Engineer: Marco Chen

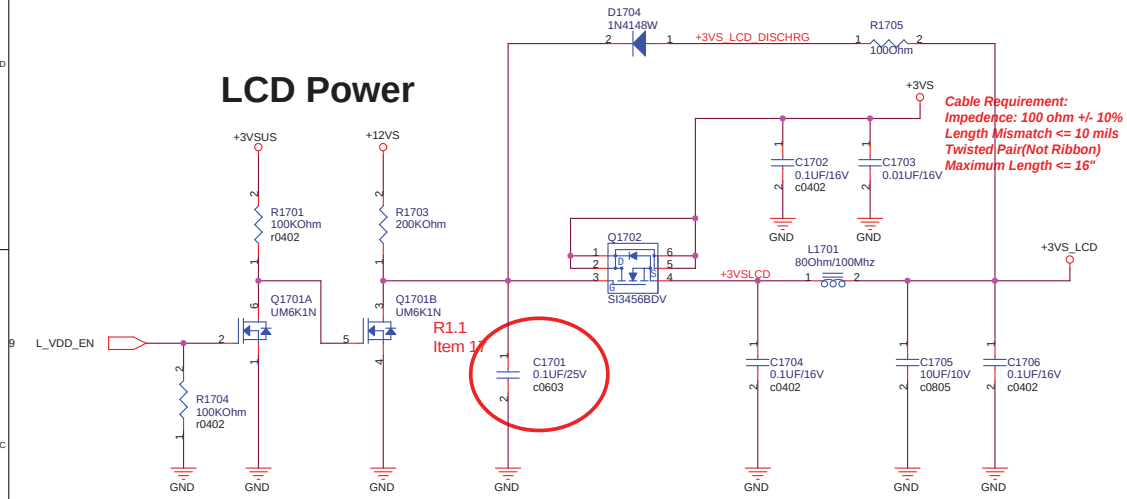
Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 16 of 63

http://laptop-motherboard-schematic.blogspot.com/

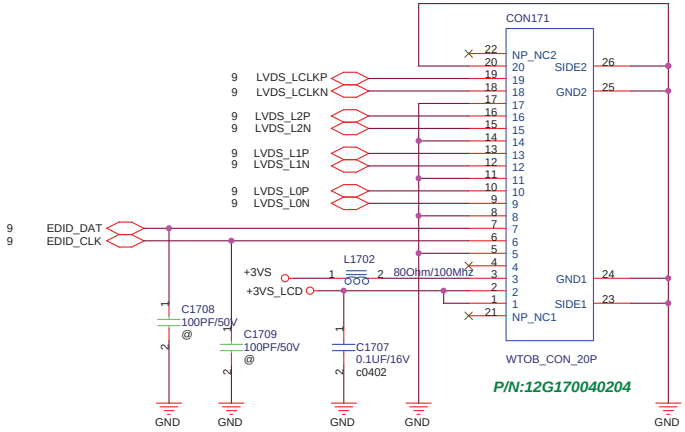
LCD Backlight Control

LCD Power

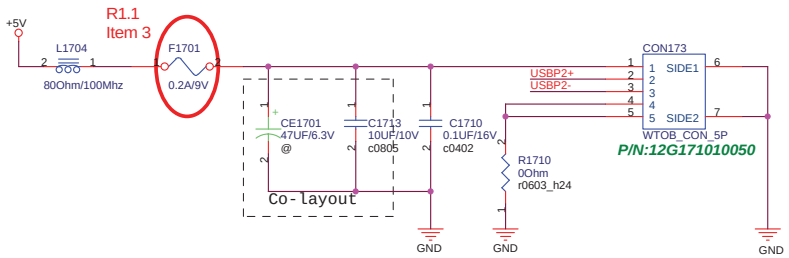


PR_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

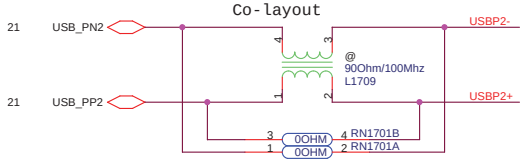
LCD LVDS Interface



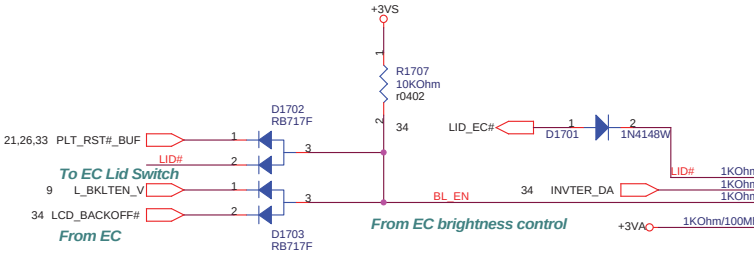
CCD connecter



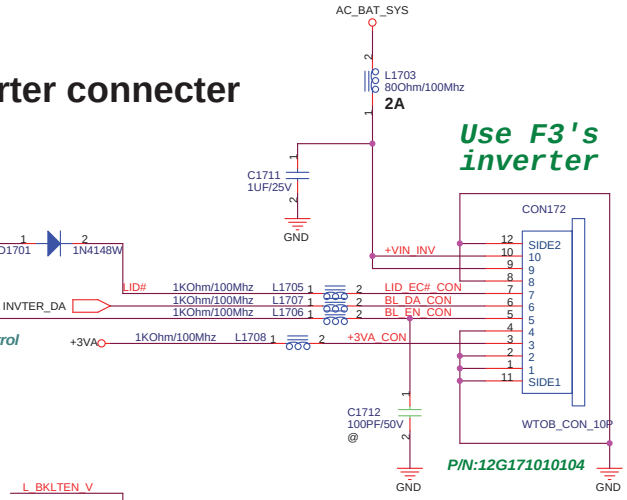
FOR EMI
Co-layout

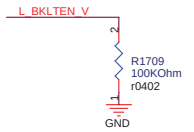


Inverter connecter



BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



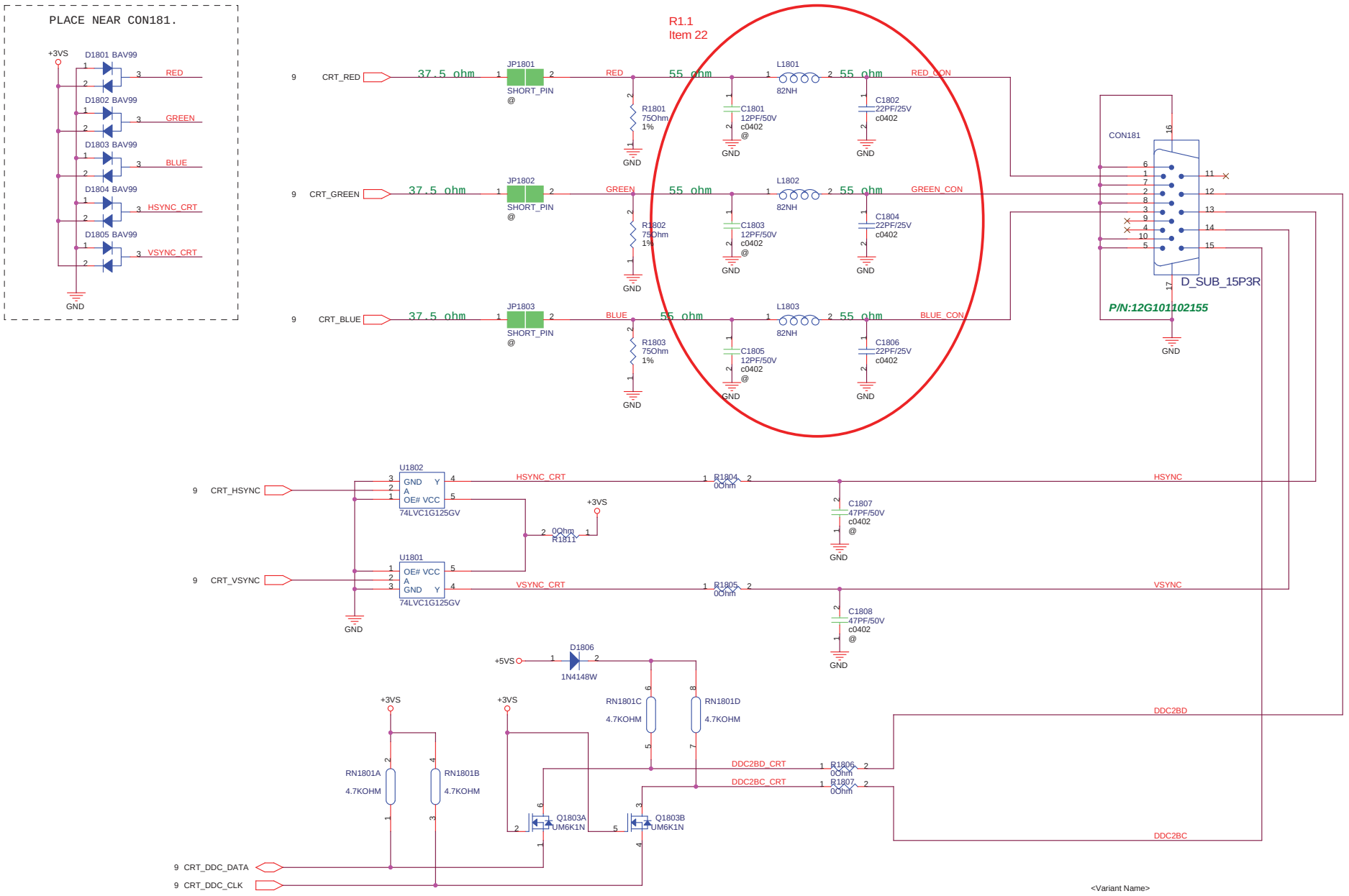


<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 17 of 63	

http://laptop-motherboard-schematic.blogspot.com/

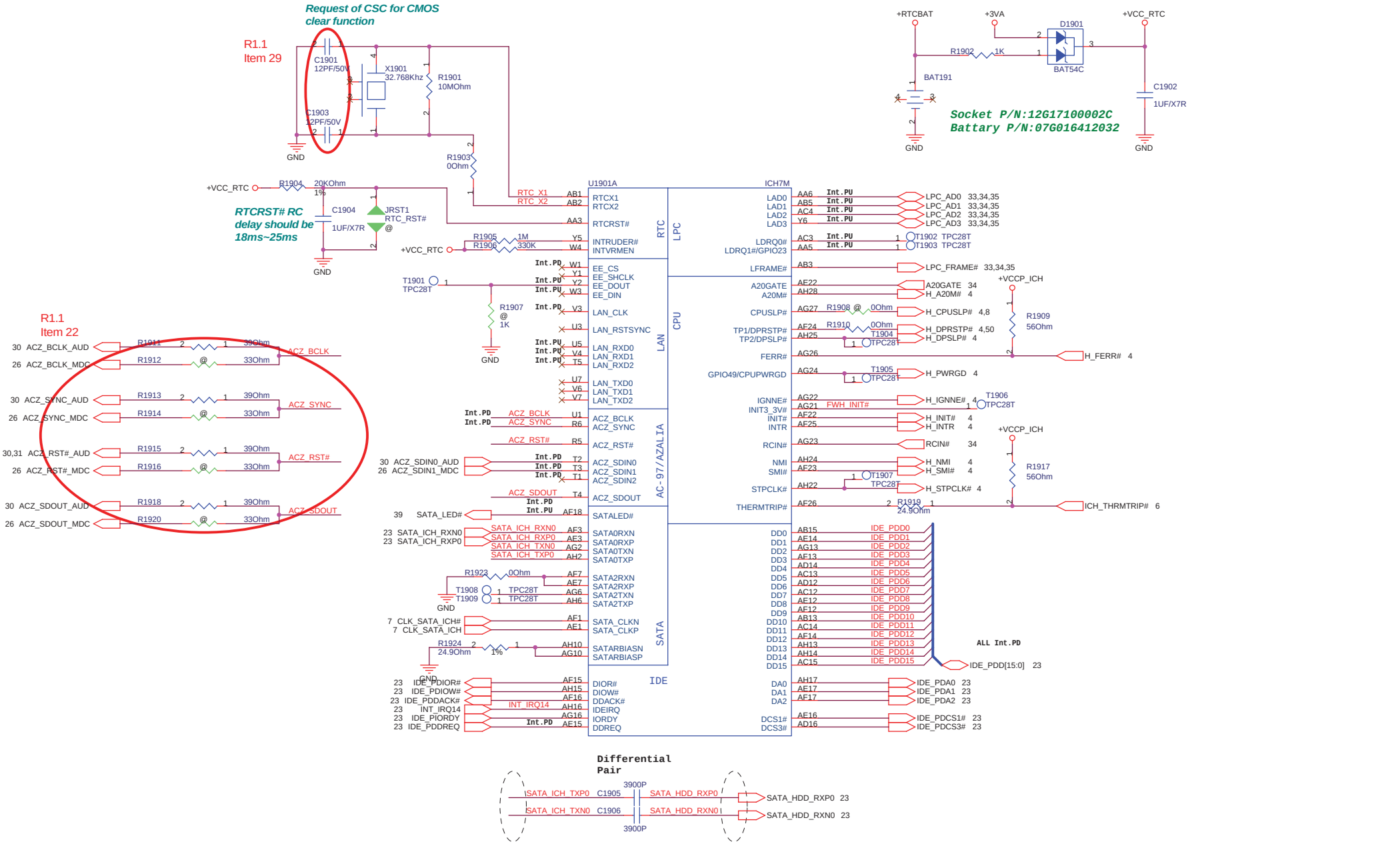
CRT



<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT CONN	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 18 of 63	

http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7M (1)

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 19 of 63

http://laptop-motherboard-schematic.blogspot.com/

To new card check power plane

Clock Generator
DDR2 SO-DIMM

U1901C — ICH7M

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1
SATA CLK: GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA2GP, GPIO37/SATA3GP
Clocks: CLK14, CLK48, SUSCLK
SYS GPIO / Power MGT: RI#, SPKR, SUS_STAT#, SYS_RST#, GPIO0/BM_BUSY#, SMBALERT#/GPIO11, GPIO18/STPPCI#, GPIO20/STPCPU#, GPIO26, GPIO27, GPIO28, GPIO32/CLKRUN#, GPIO33/AZ_DOCK_EN#, GPIO34/AZ_DOCK_RST#, WAKE#, SERIRQ, THRM#, VRMPWRGD, GPIO6, GPIO7, GPIO8
GPIO: SLP_S3#, SLP_S4#, SLP_S5#, PWROK, GPIO16/DPRSLPVR, TP0/BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, GPIO24, GPIO25, GPIO35, GPIO38, GPIO39

7,14,15,33 SCL_3S
7,14,15,33 SDA_3S
LINKALERT#
SM_LINK0
SM_LINK1
RING#
30 SPKR_ICH — T2007 TPC28T — PM_SUS_STAT# — 10KOhm R2001 — +3VSUS
9 PM_BMBUSY#
SMB_ALERT#
7 STP_PCI#
7 STP_CPU#
25 BT_ON#
26 WLAN_ON#
35 MEMROM/YONAH# — T2018 TPC28T
27 PM_CLKRUN#
T2014 TPC28T
7 CPU_Select
26,29,33 PCIE_WAKE#
27,34 INT_SERIRQ
34 PM_THRM#
T2001 TPC28T — VRMPWRGD
34,50,60 VRM_PWRGD — R2004 0Ohm
39 BT_LED_EN — T2017 TPC28T
34 EXTSMI#

R1.1
Item 12

VRM_PWRGD
Pull Hi 100K
+3Vs at power circuit

POWER

AF19 — T2009 TPC28T
AH18 — T2010 TPC28T
AH19 — T2008 TPC28T
AE19 PCB_ID0

AC1, B2 — CLK_ICH14 7, CLK_USB48 7
C20 SUS_CLK — T2005 TPC28T
C2001 @ 10PF/50V, C2002 @ 10PF/50V — GND, GND

B24 SLP_S3# — SUSB# 34
D23 SLP_S4# — SUSC# 34
F22 — T2002 TPC28T

AA4 PWROK — ICH7_PWROK 9,27,34
AC22 Int.PD — POWER — PM_DPRSLPVR 50
C21 BAT_LL# 34
C23 Int.PU — T2003 TPC28T — PM_PWRBTN# 34
R2002 10KOhm — GND
C19 ICH_LAN_RST# — R2036 0Ohm
Y4 RSMRST# — PM_RSMRST# 34
R2030 10KOhm — GND

E20 — T2016 TPC28T
A20 — T2011 TPC28T
F19 KBC_SCI# 34
E19 — T2004 TPC28T
R4 — T2012 TPC28T
F22 802_LED_EN 39
R3 MSK_PCIRST 21
D20 Int.PU
AD21 — T2013 TPC28T
AD20 PCB_ID1
AE20 PCB_ID2

+3VS
21,27 PCI_SERR# — RP2001A 1 8.2KOhm 5 10
21,27 PCI_DEVSEL# — RP2001B 2 8.2KOhm 5 10
21,27 PCI_TRDY# — RP2001C 3 8.2KOhm 5 10
21 PCI_REQ#4 — RP2001D 4 8.2KOhm 5 10
21,27 PCI_FRAME# — RP2001E 6 8.2KOhm 5 10
21,27 PCI_STOP# — RP2001F 7 8.2KOhm 5 10
21,27 PCI_REQ#1 — RP2001G 8 8.2KOhm 5 10
21 PCI_REQ#2 — RP2001H 9 8.2KOhm 5 10

RP2002A 1 8.2KOhm 5 10
21 PCI_REQ#3 — RP2002B 2 8.2KOhm 5 10
21 PCI_LOCK# — RP2002C 3 8.2KOhm 5 10
RP2002D 4 8.2KOhm 5 10
21 PCI_INTH# — RP2002E 6 8.2KOhm 5 10
21 PCI_INTF# — RP2002F 7 8.2KOhm 5 10
21 PCI_INTE# — RP2002G 8 8.2KOhm 5 10
21 PCI_INTG# — RP2002H 9 8.2KOhm 5 10

21 PCI_INTA# — RP2003A 1 8.2KOhm 5 10
21,27 PCI_INTB# — RP2003B 2 8.2KOhm 5 10
21 PCI_INTC# — RP2003C 3 8.2KOhm 5 10
21,27 PCI_INTD# — RP2003D 4 8.2KOhm 5 10
21 PCI_REQ#0 — RP2003E 6 8.2KOhm 5 10
21,27 PCI_IRDY# — RP2003F 7 8.2KOhm 5 10
21 PCI_REQ#5 — RP2003G 8 8.2KOhm 5 10
21,27 PCI_PERR# — RP2003H 9 8.2KOhm 5 10

INT_SERIRQ — R2013 10KOhm
STP_PCI# — R2015 @ 10KOhm
STP_CPU# — R2020 @ 10KOhm
PM_CLKRUN# — R2023 10KOhm

ICH7_PWROK — R2006 @ 0Ohm — VRMPWRGD

+3VS
SCL_3S — R2005 2.2KOhm
SDA_3S — R2007 2.2KOhm
PM_THRM# — R2026 10KOhm

+3VSUS
RING# — R2008 10KOhm
SMB_ALERT# — RN2001A 1 10KOhm 2
SM_LINK0 — RN2001B 3 10KOhm 4
SM_LINK1 — RN2001C 5 10KOhm 6
LINKALERT# — RN2001D 7 10KOhm 8
BAT_LL# — R2014 10KOhm
WLAN_ON# — R2016 10KOhm
PCIE_WAKE# — R2021 2.2KOhm
PM_SUS_STAT# — R2025 @ 10KOhm
BT_ON# — R2028 10KOhm

+3VS
PCB_ID0 — R2009 10KOhm
PCB_ID1 — R2010 10KOhm @
PCB_ID2 — R2011 10KOhm @
R2017 10KOhm @ — GND
R2018 10KOhm — GND
R2019 10KOhm — GND

+3VSUS
KBC_SCI# — R2034 10KOhm
EXTSMI# — R2035 10KOhm

R1.1
Item 12
MEMROM/YONAH# — R2033 10KOhm
802_LED_EN — R2031 10KOhm
BT_LED_EN — R2032 10KOhm
GND

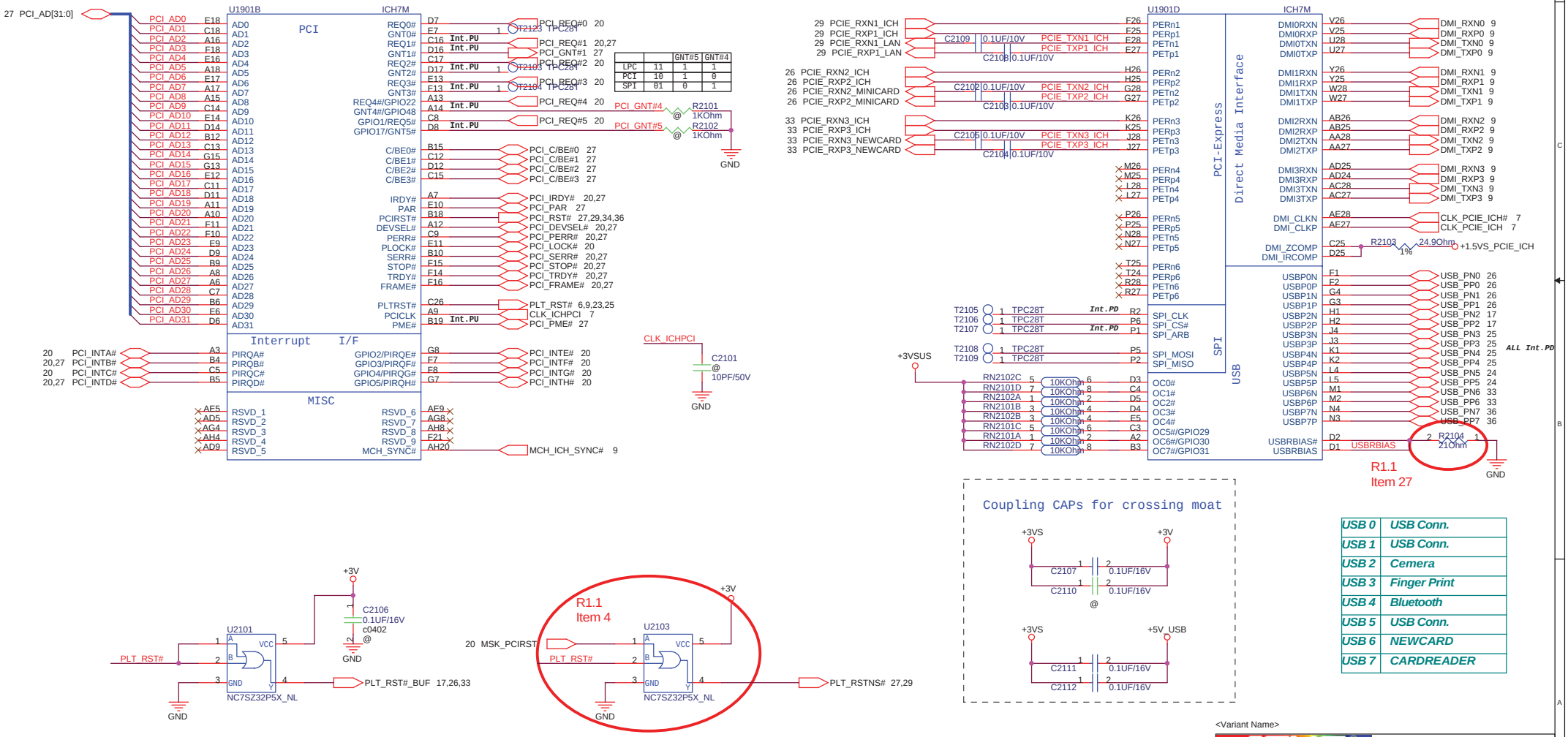
<Variant Name>

ASUSTeK COMPUTER INC
Title : ICH7M (2)
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 20 of 63

http://laptop-motherboard-schematic.blogspot.com/



		GNT#5	GNT#4
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER

<Variant Name>

ASUSTeK COMPUTER INC

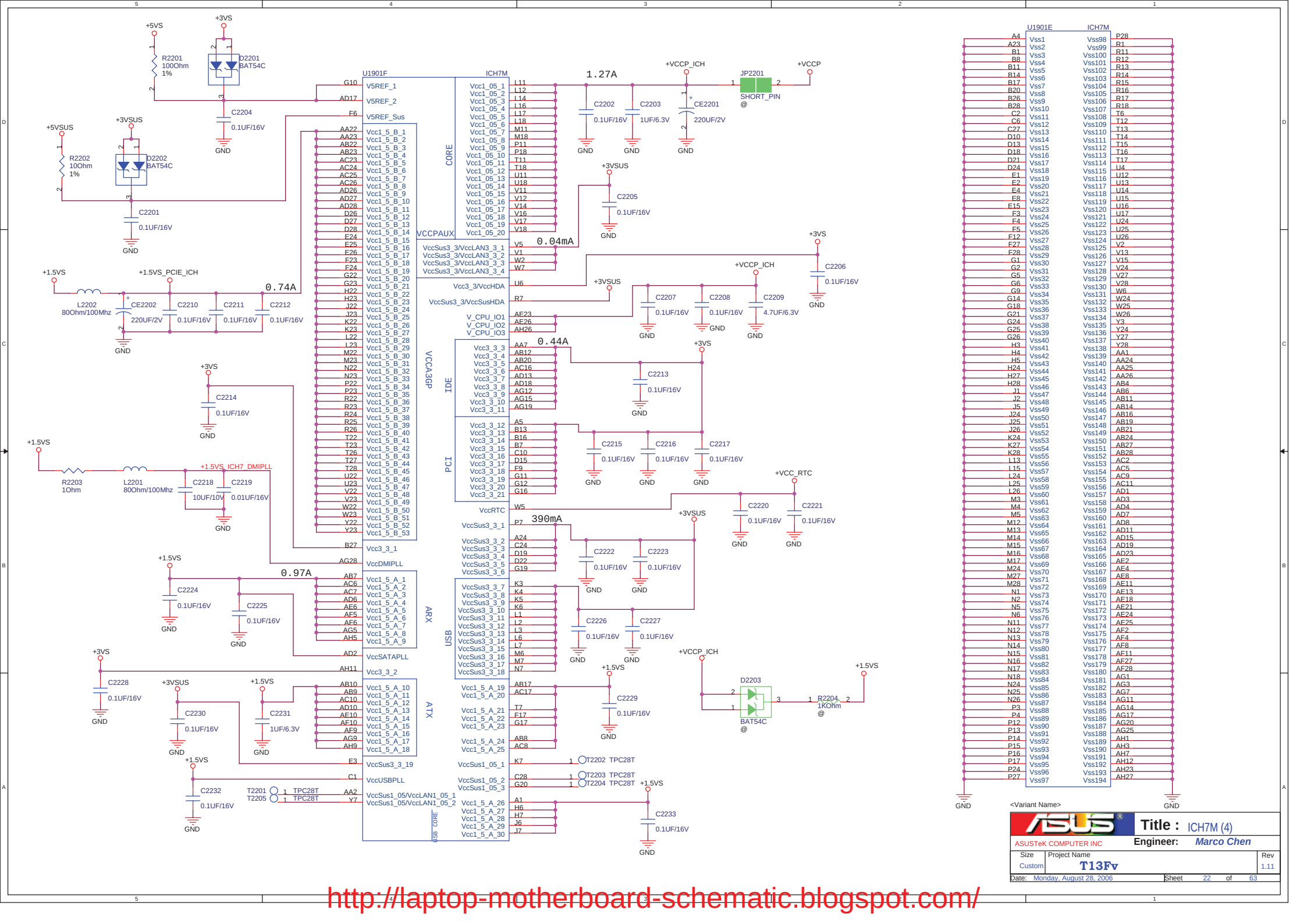
Title : ICH7M (3)

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

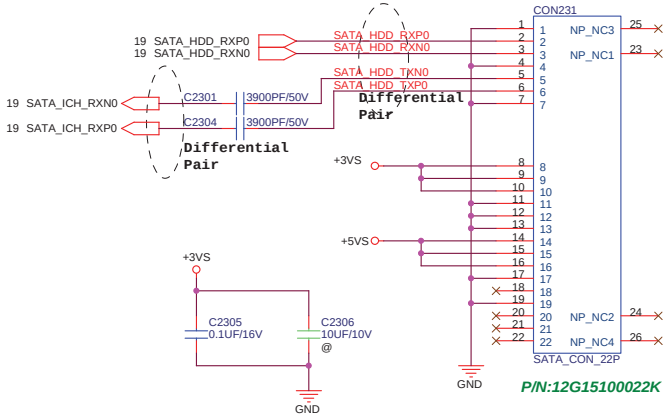
Date: Monday, August 28, 2006 Sheet 21 of 63

http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

SATA HDD CON



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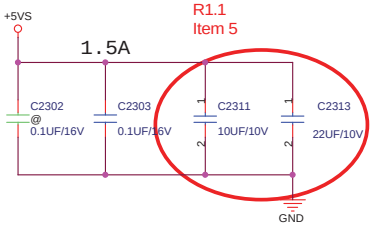
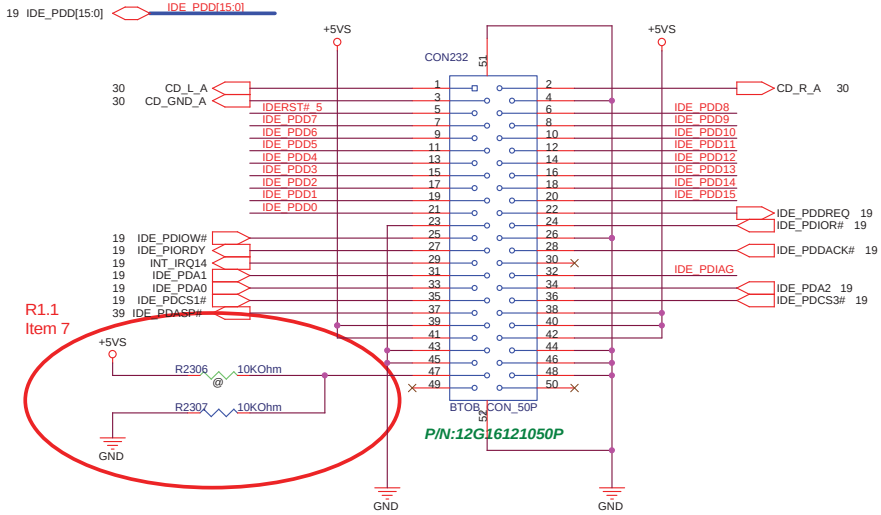


PATA ODD CON



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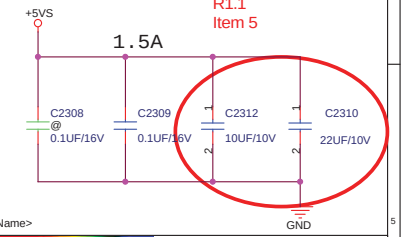

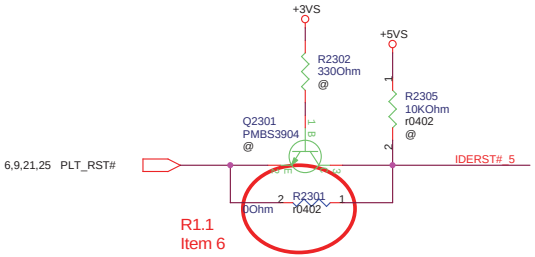

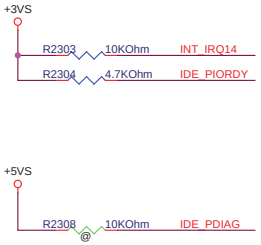

Normal type
High: Slave
Low : Master

<Variant Name>

Title : HDD & ODD

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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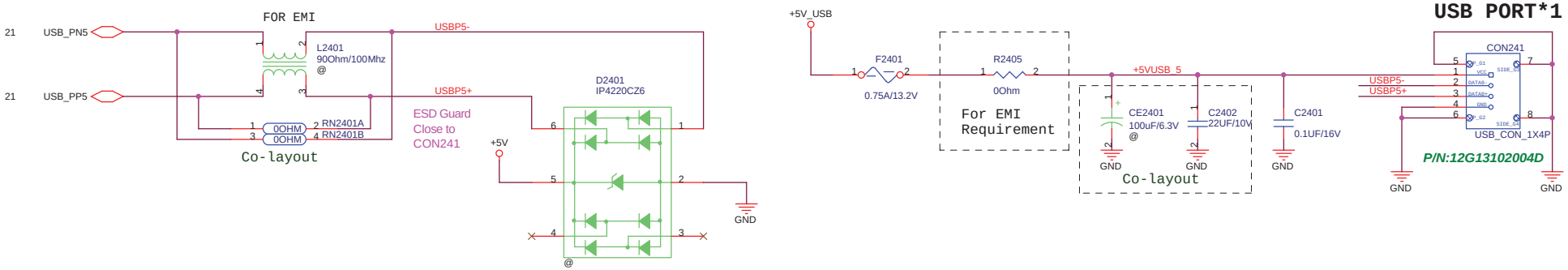
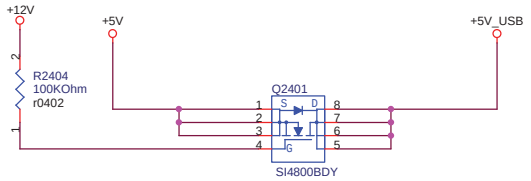
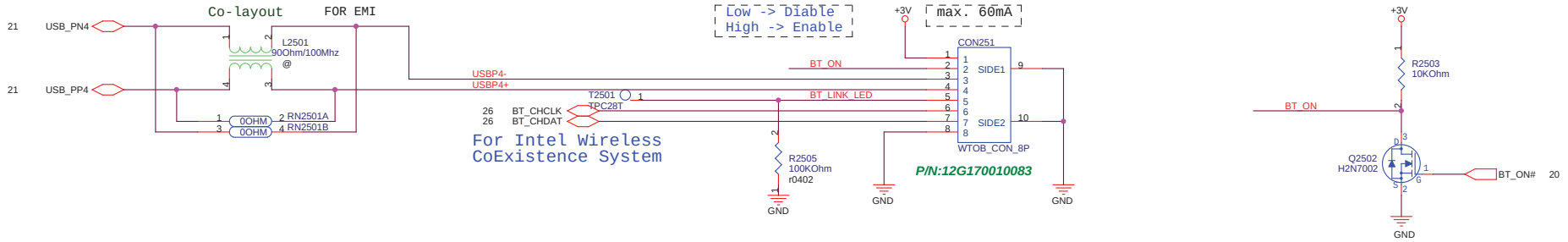




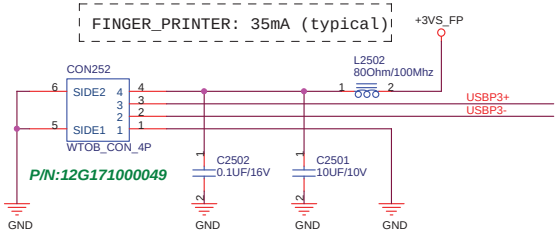
<Variant Name>

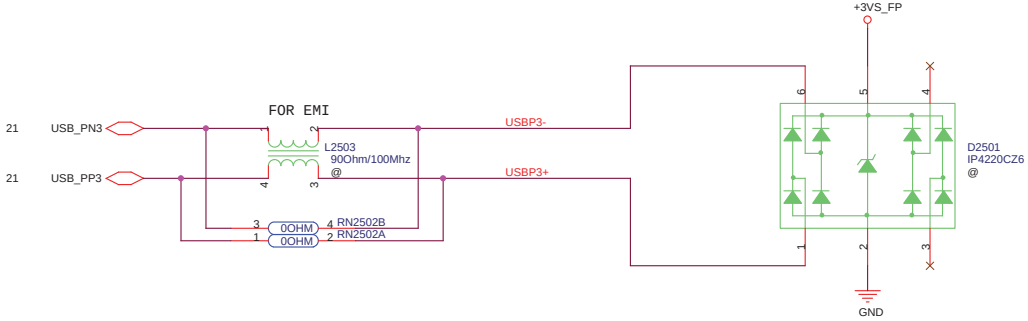
ASUSTeK COMPUTER INC	Title : USB PORT	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 24 of 63	

http://laptop-motherboard-schematic.blogspot.com/

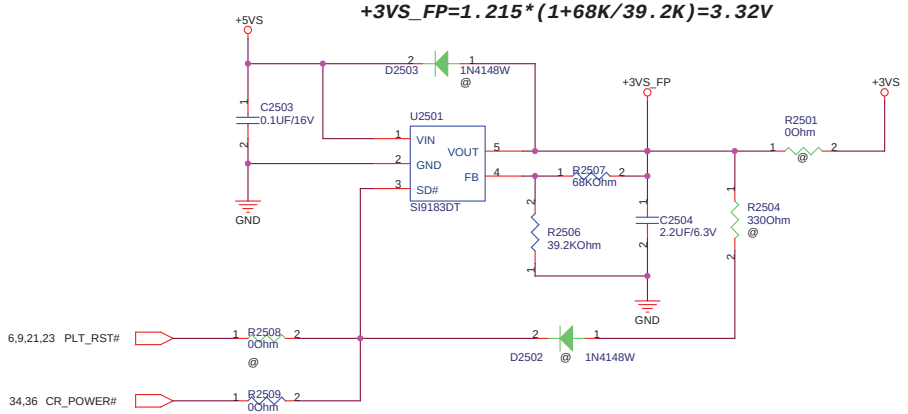


Finger Printer





+3VS_FP=1.215*(1+68K/39.2K)=3.32V



<Variant Name>

ASUSTeK COMPUTER INC	Title : BT & FP	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 25 of 63	

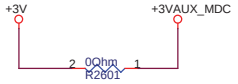
http://laptop-motherboard-schematic.blogspot.com/

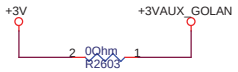
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

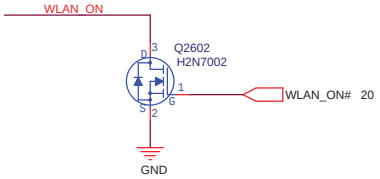
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

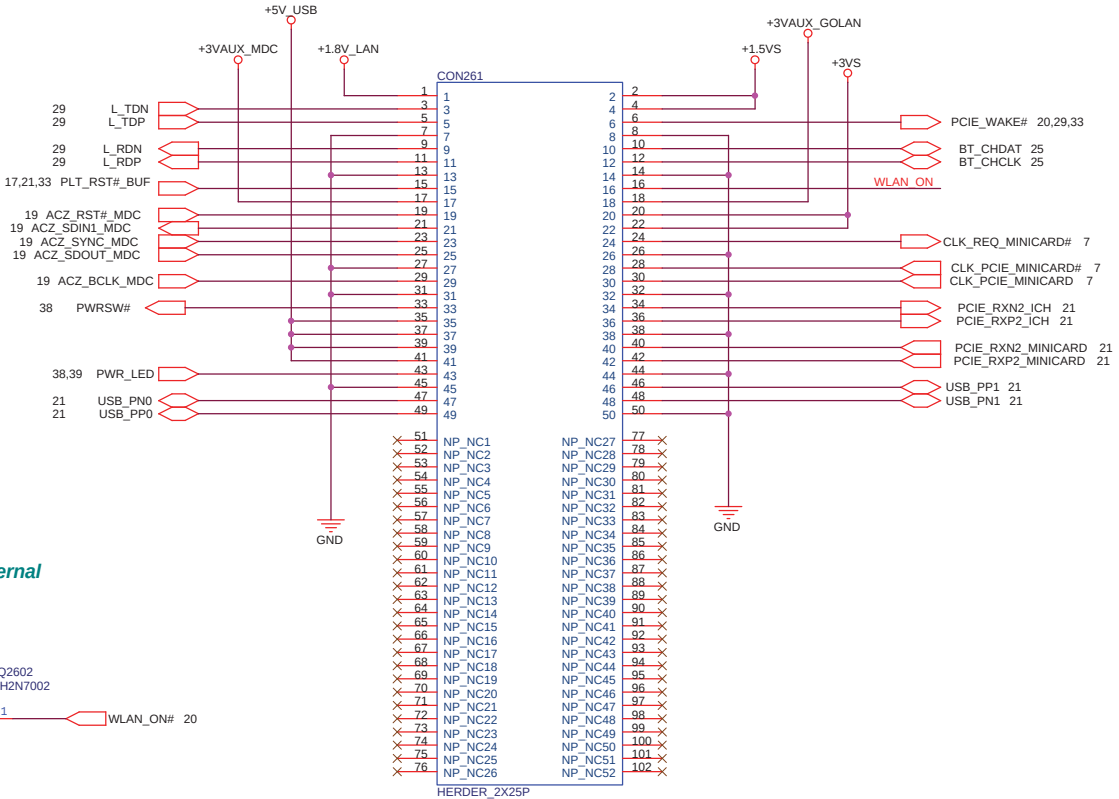
+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA





Intel SPEC(18780):Internal
Pull UP 110Kohm



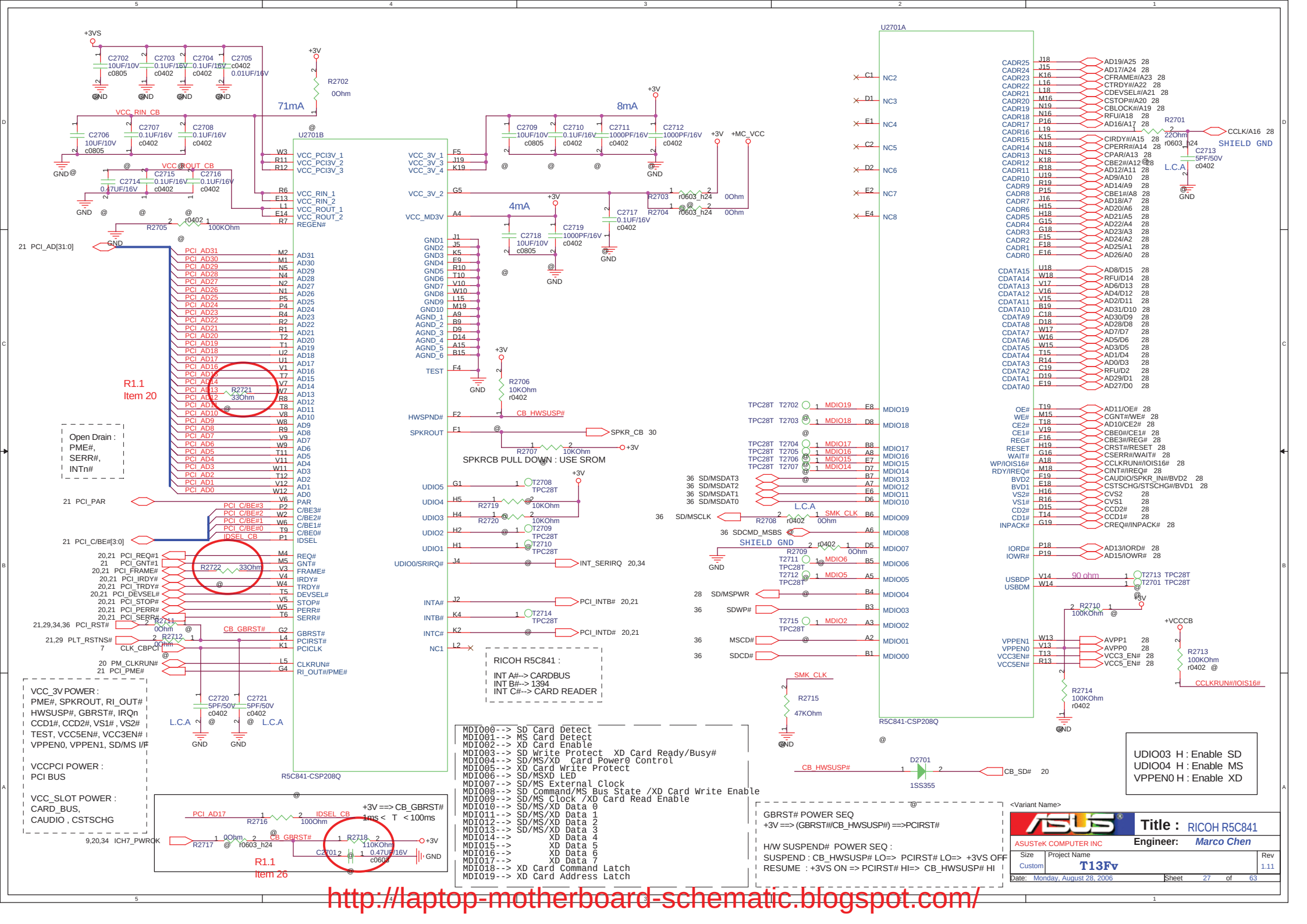


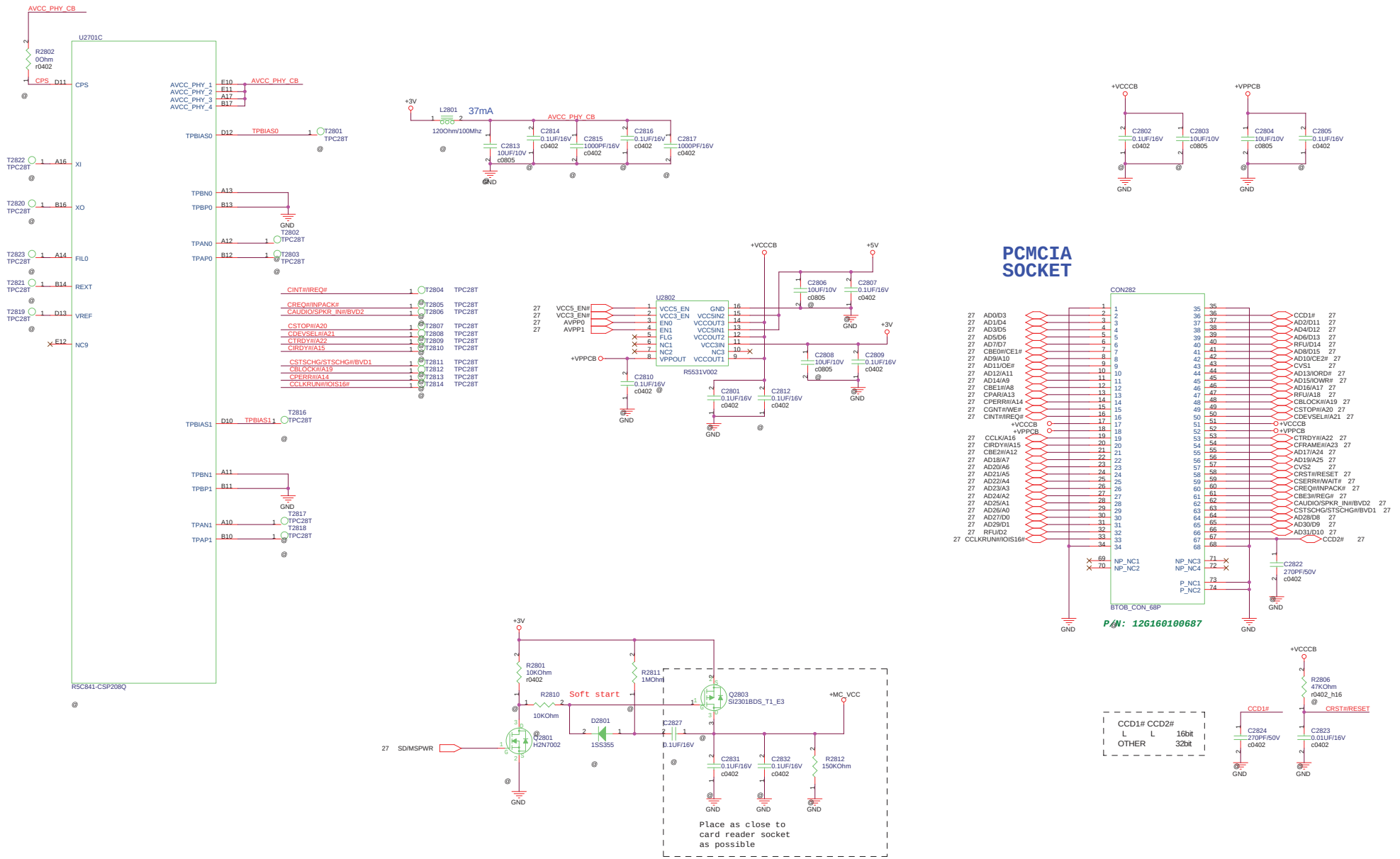
P/N:12G061200504

<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 26 of 63	

http://laptop-motherboard-schematic.blogspot.com/

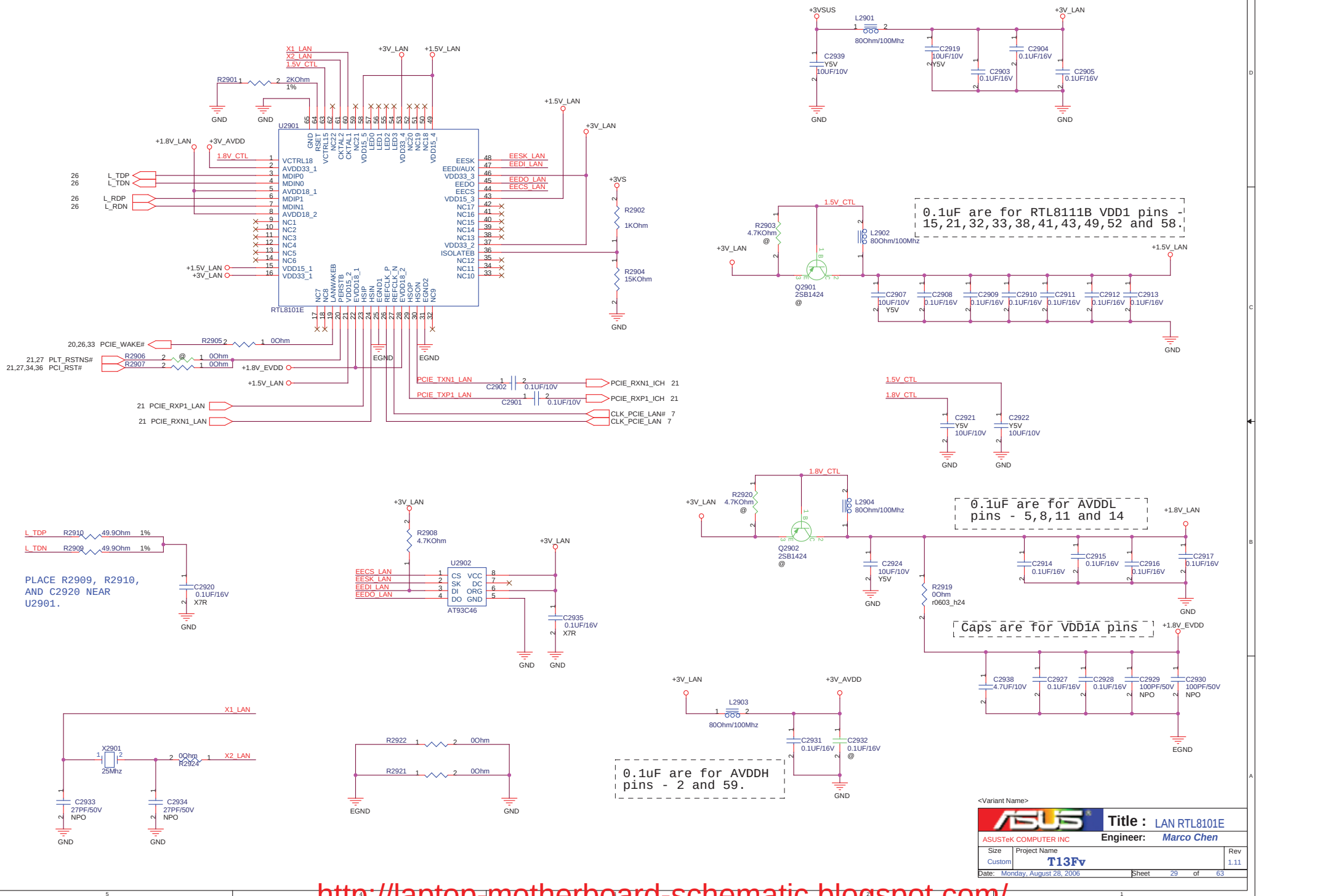

U2701A
R5C841-CSP208Q
U2701B
R5C841-CSP208Q
71mA
8mA
4mA
R1.1
Item 20
R1.1
Item 26
Open Drain :
PME#,
SERR#,
INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 27 of 63
http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

ASUSTeK COMPUTER INC	Title : PCMCIA&3IN1 SOCKET	
	Engineer: Marco Chen	
Size: C	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 28 of 63	

http://laptop-motherboard-schematic.blogspot.com/



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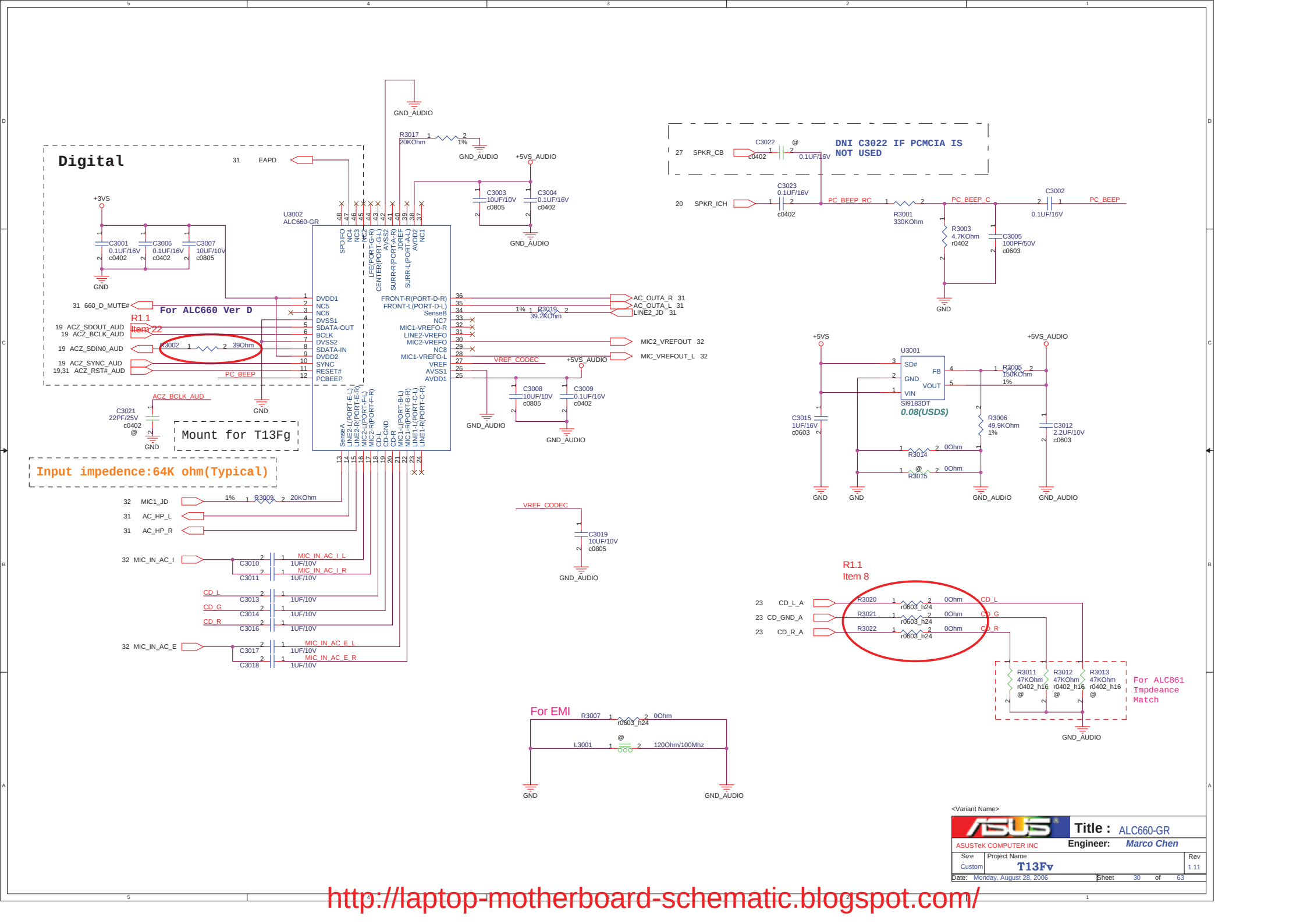
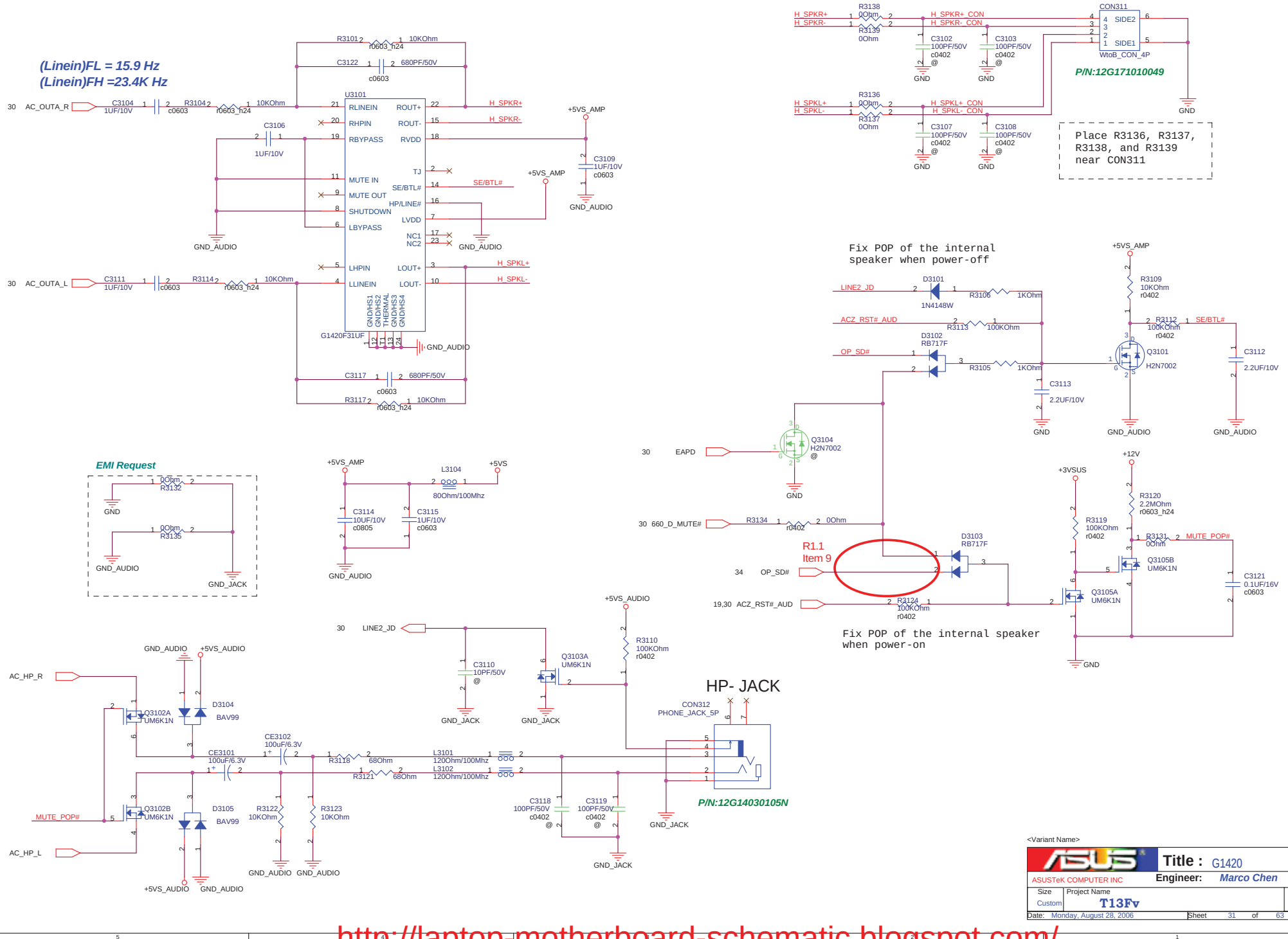


http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

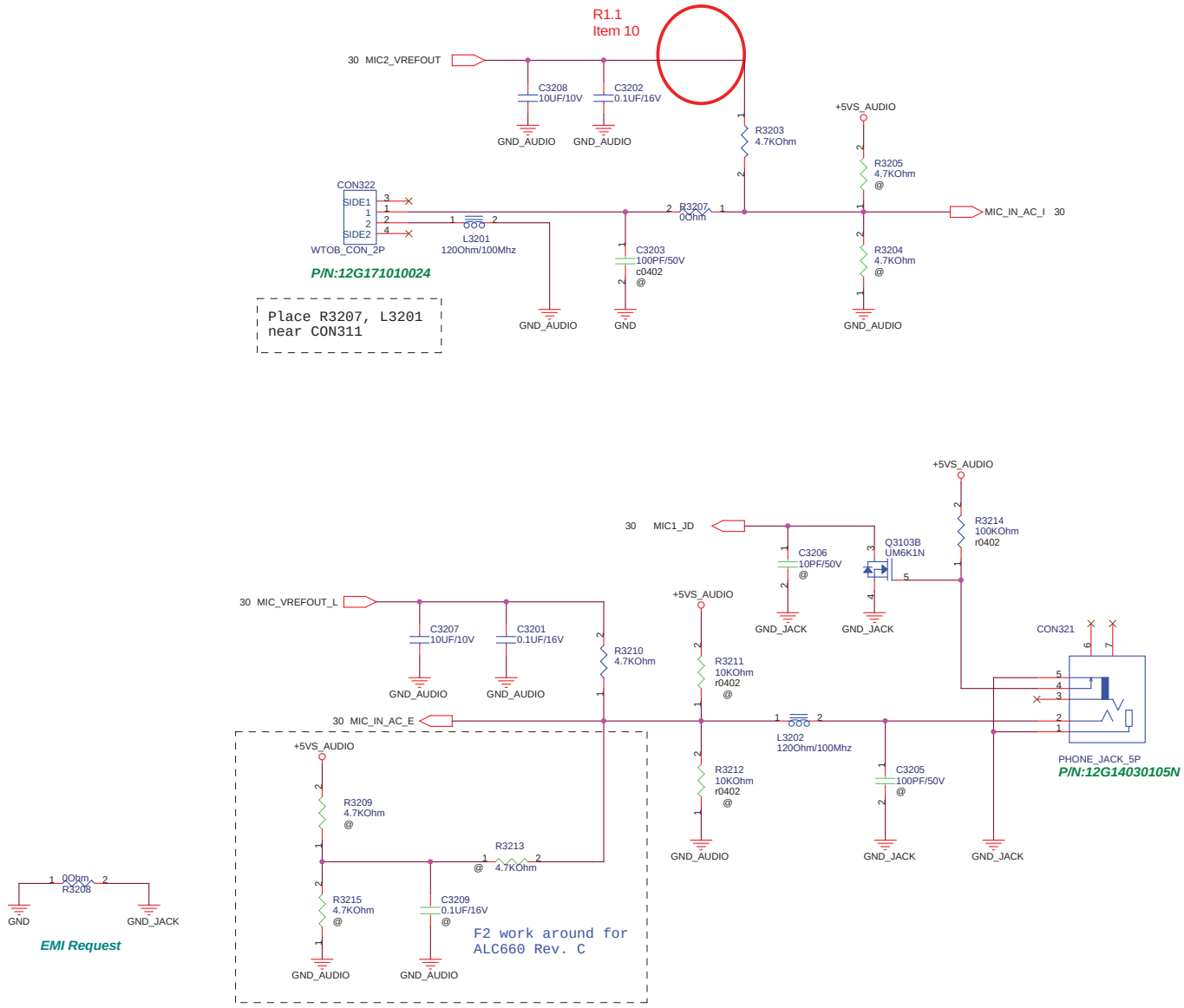
<Variant Name>

Title : G1420

ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

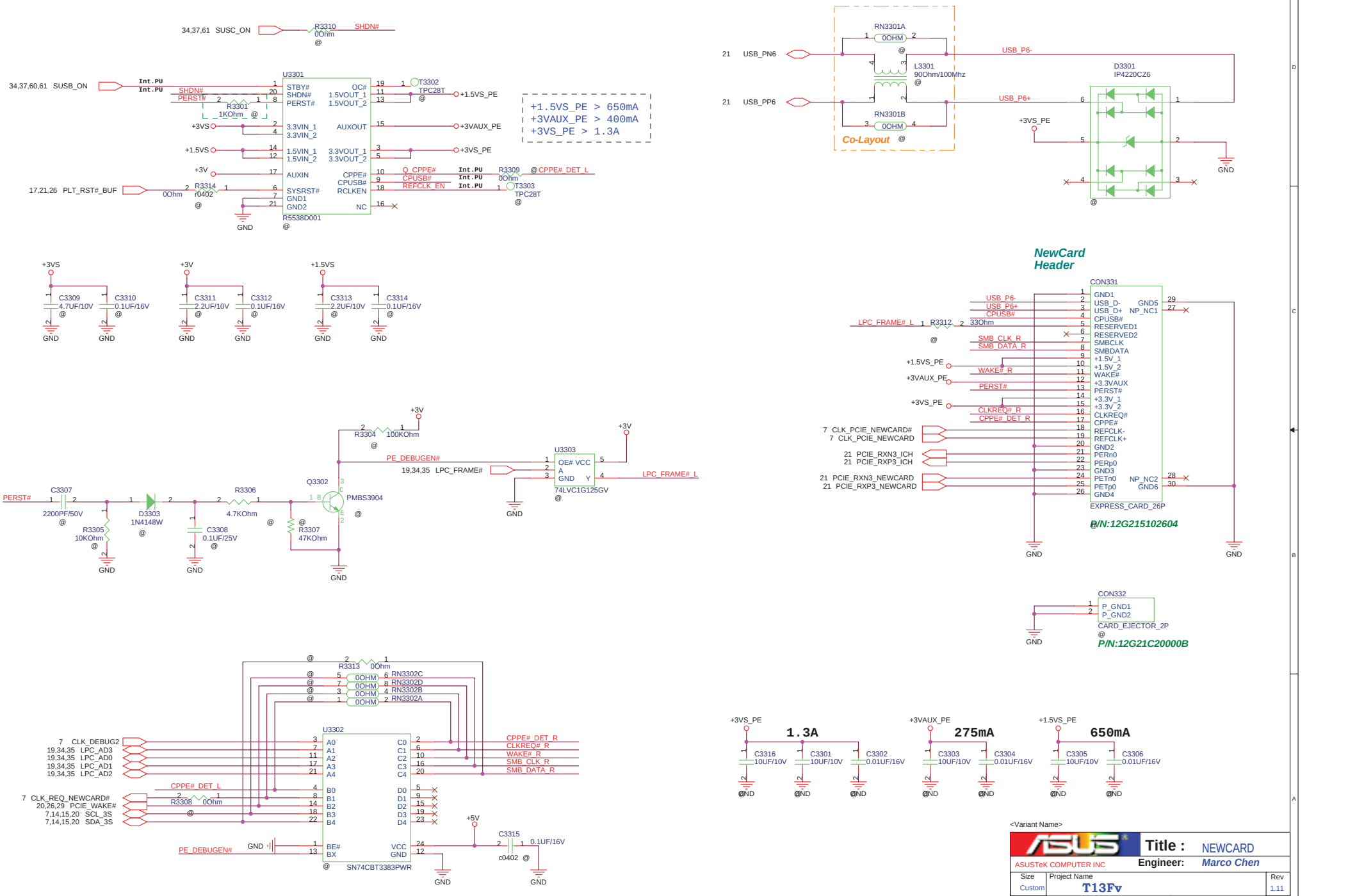
Date: Monday, August 28, 2006 Sheet 31 of 63



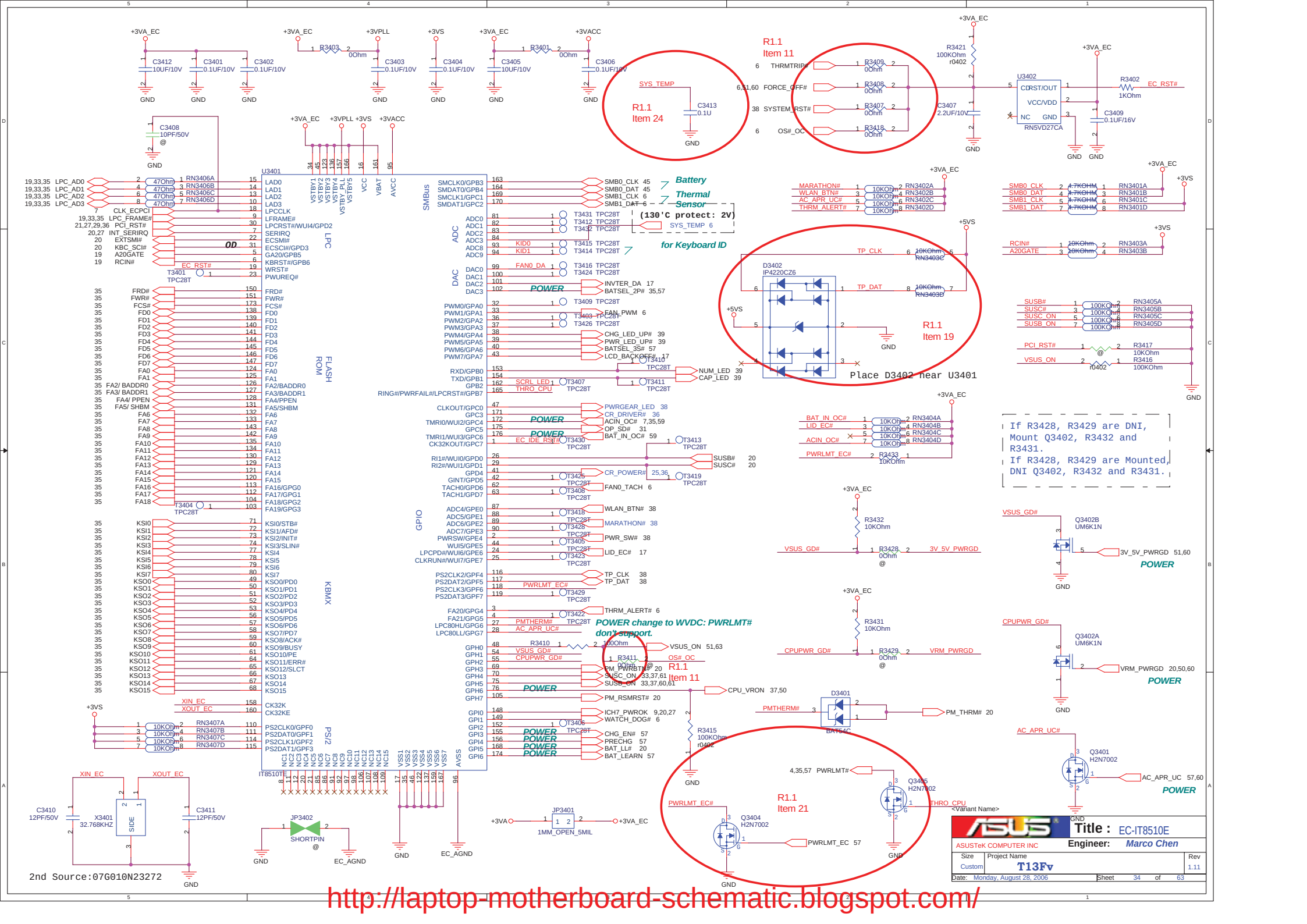
<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 32 of 63	

http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

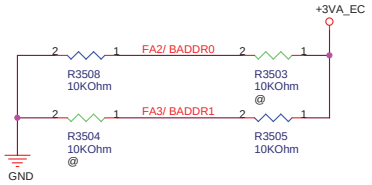


http://laptop-motherboard-schematic.blogspot.com/

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

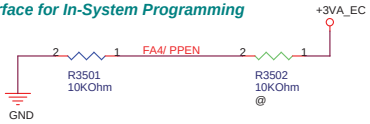
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

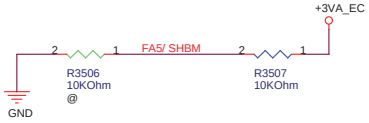
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

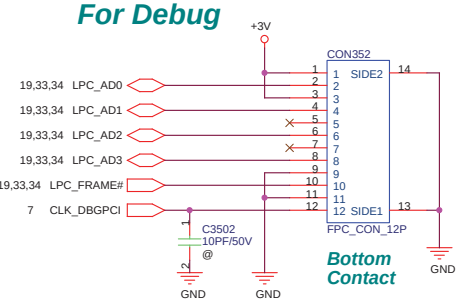


FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

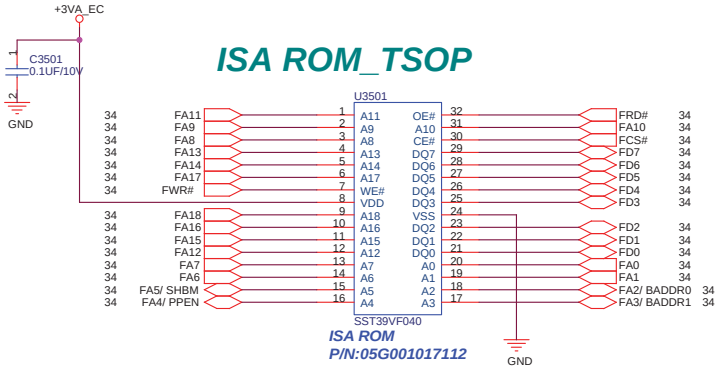


For Debug

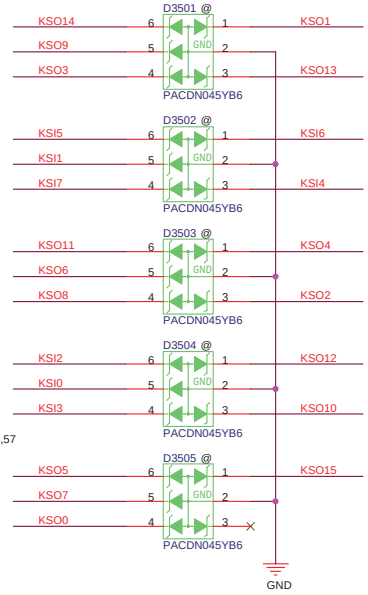


P/N:12G183301208

ISA ROM_TSOP

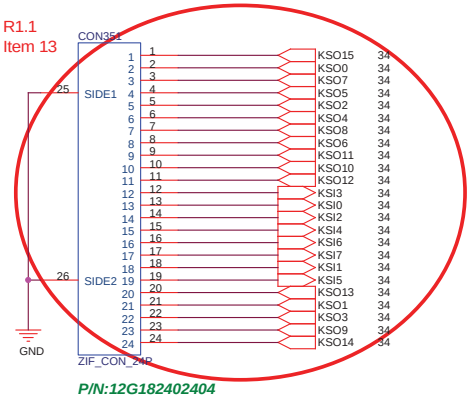


ISA ROM
P/N:05G001017112



For Keyboard

R1.1
Item 13



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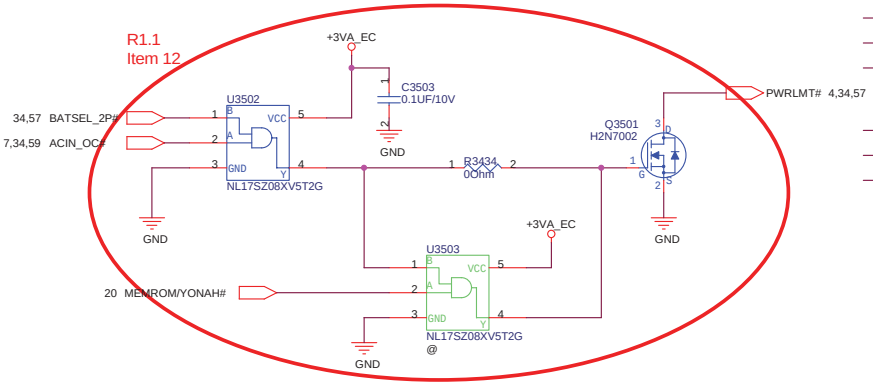
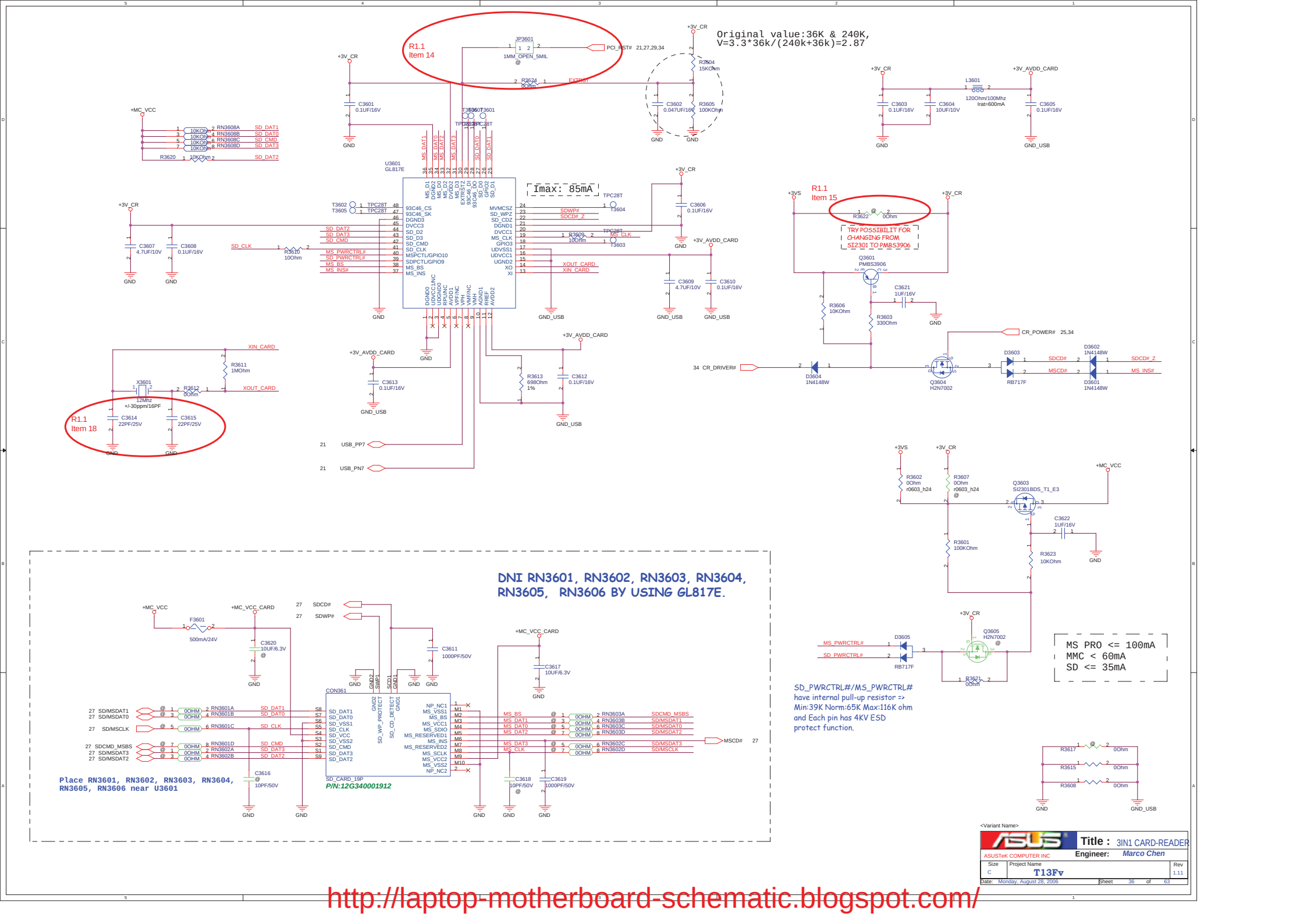
R1.1
Item 12



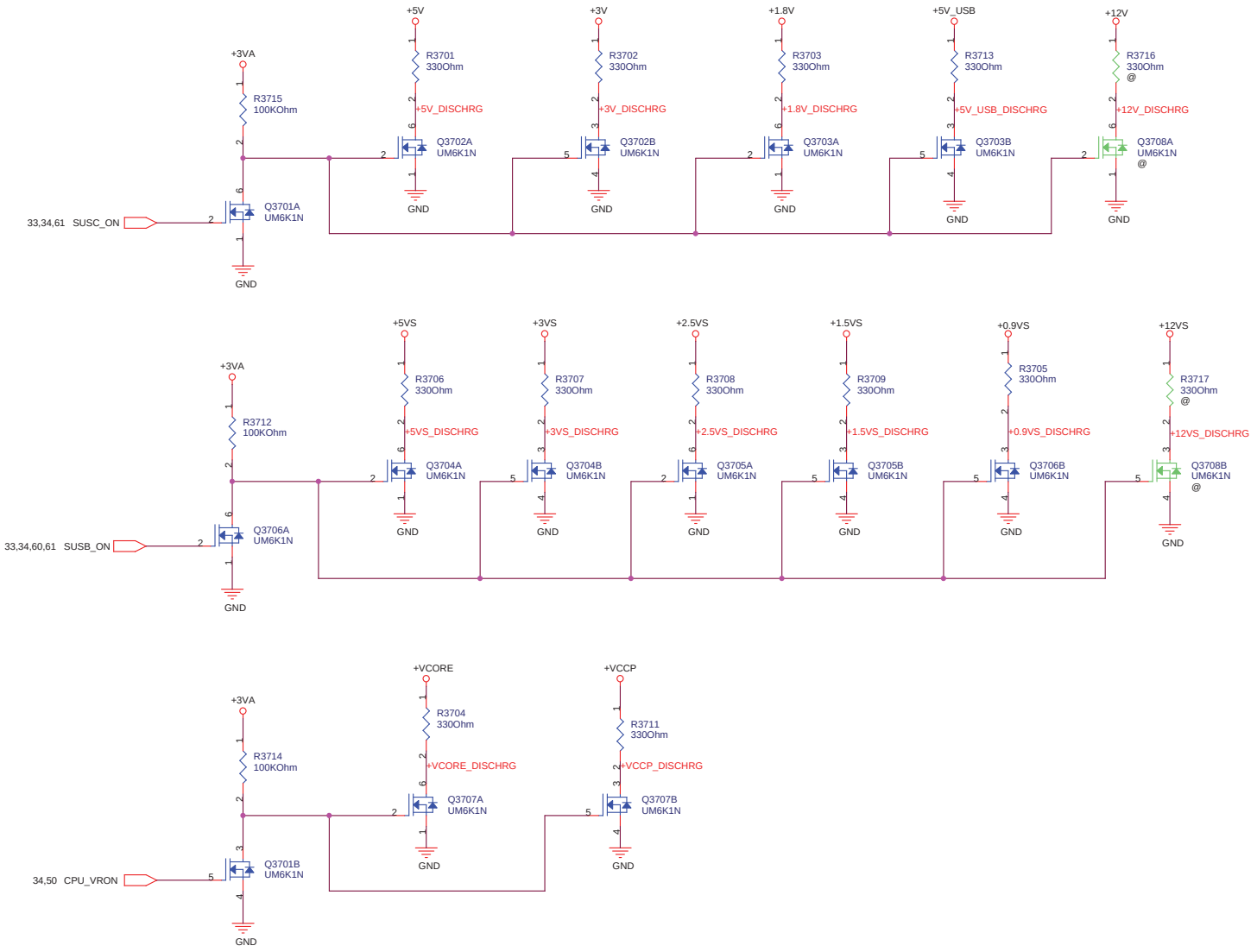
<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 35 of 63	

http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

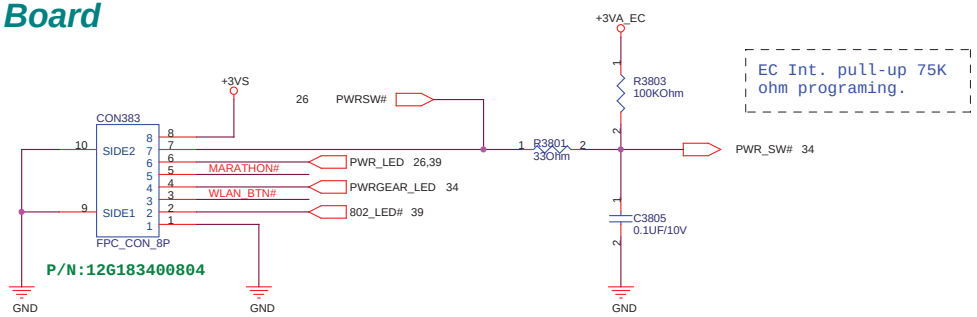


<Variant Name>

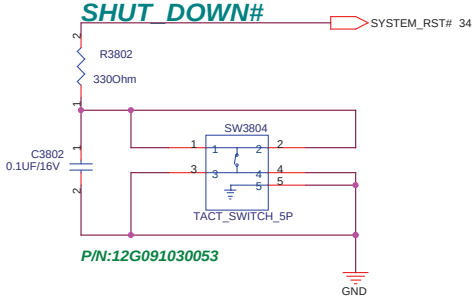
ASUSTeK COMPUTER INC	Title : DISCHARGE	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 37 of 63	

http://laptop-motherboard-schematic.blogspot.com/

FFC CONNECTER for T13Fv SW Board

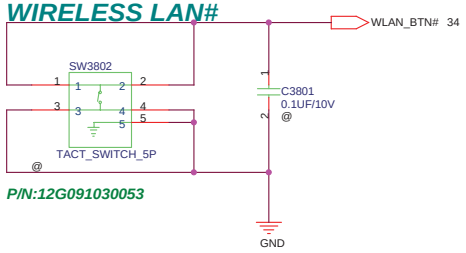


SHUT_DOWN#

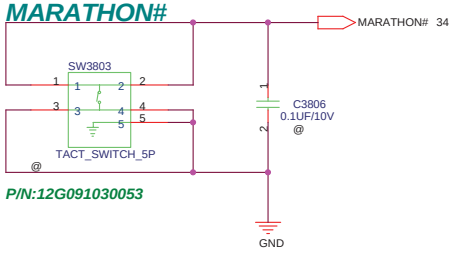


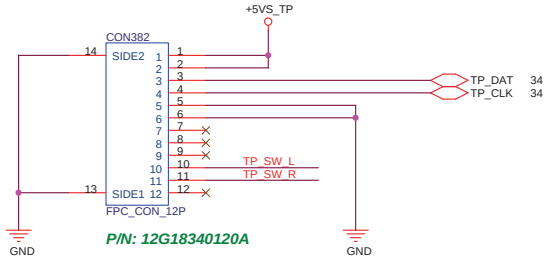
INSTANT KEY for T13Fg

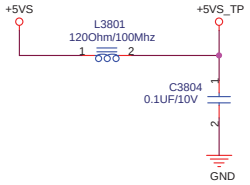
WIRELESS LAN#



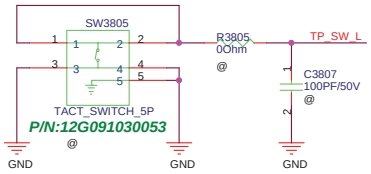
MARATHON#

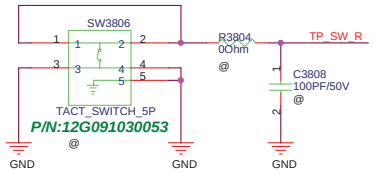






Select Button for T13Fg





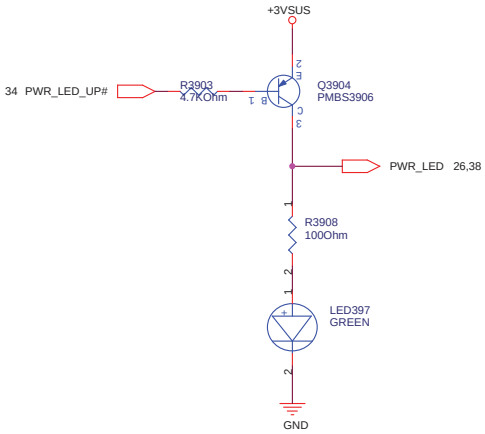
<Variant Name>

ASUSTeK COMPUTER INC	Title : Key & FFC CONN	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 38 of 63	

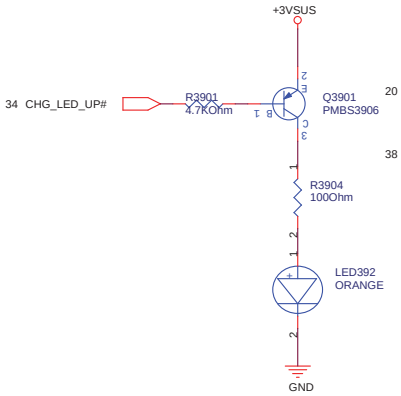
http://laptop-motherboard-schematic.blogspot.com/

PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.

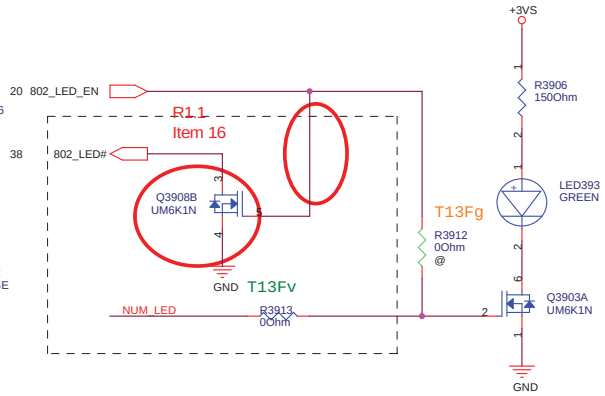
For POWER LED



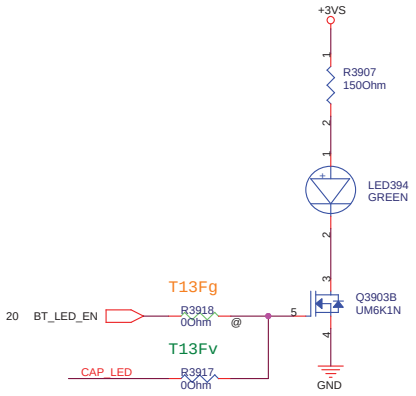
For BATTERY LED



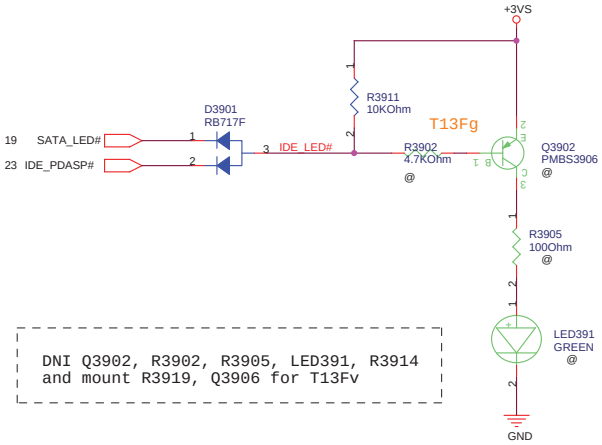
For WireLess LED



For BT LED

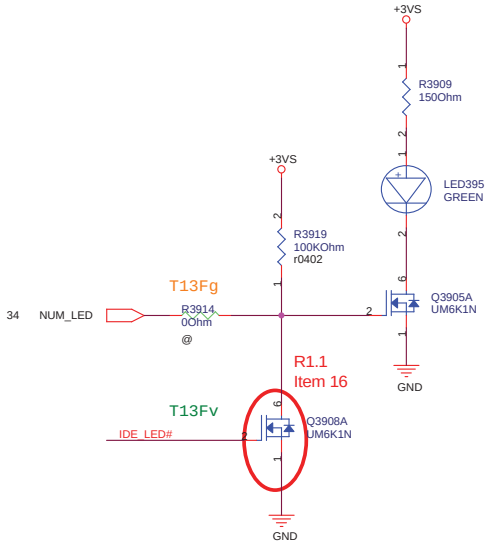


For SATA/IDE LED

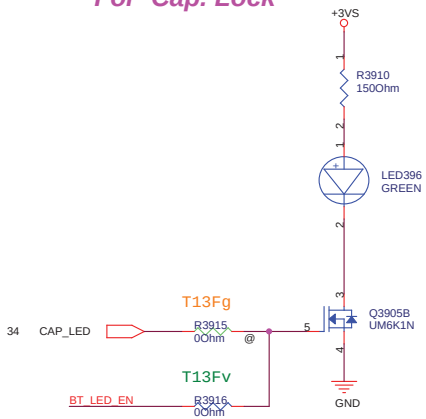


DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3906 for T13Fv

For Num Lock



For Cap. Lock



<Variant Name>

Title : LEDs

ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 39 of 63

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 40 of 63

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 41 of 63

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 42 of 63

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 43 of 63

http://laptop-motherboard-schematic.blogspot.com/

<Variant Name>

Title : EMPTY

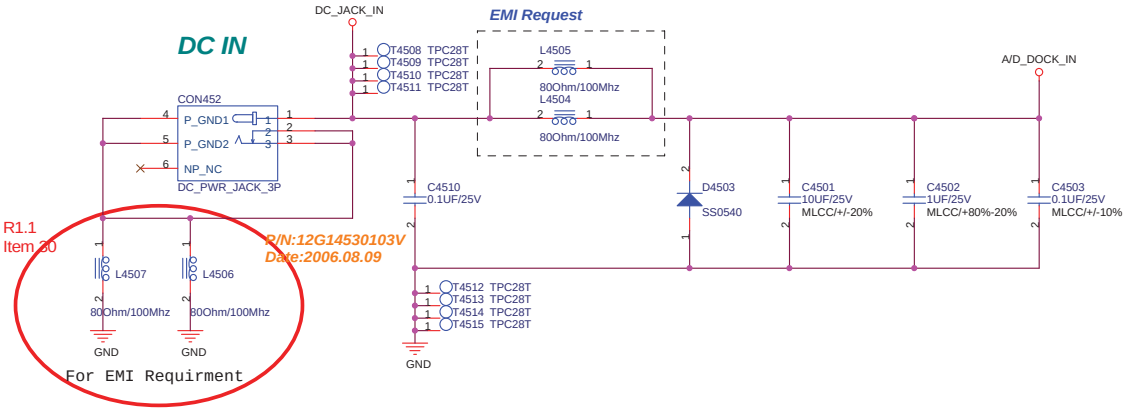
ASUSTeK COMPUTER INC

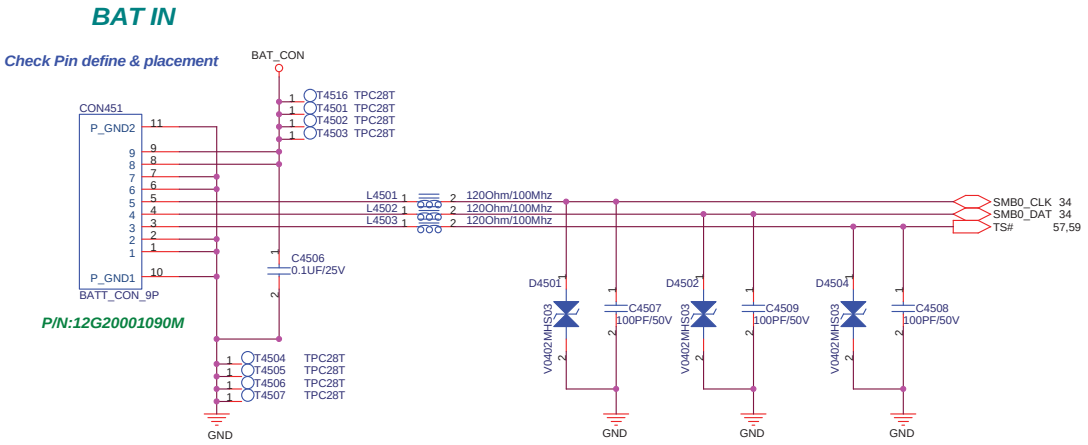
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 44 of 63

http://laptop-motherboard-schematic.blogspot.com/





<Variant Name>

ASUSTeK COMPUTER INC

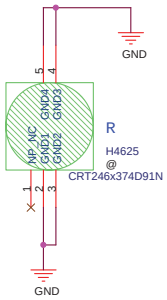
Title : BAT&Adapter conn

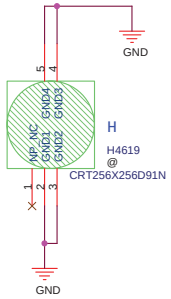
Engineer: Marco Chen

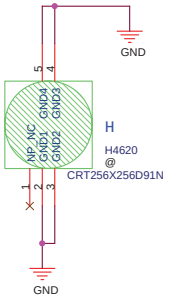
Size	Project Name	Rev
Custom	T13Fv	1.11

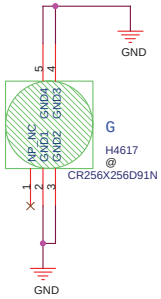
Date: Monday, August 28, 2006 Sheet 45 of 63

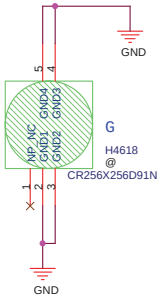
http://laptop-motherboard-schematic.blogspot.com/

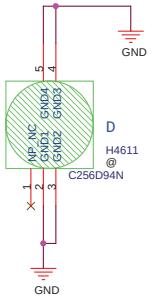


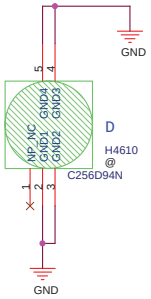


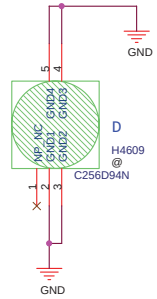


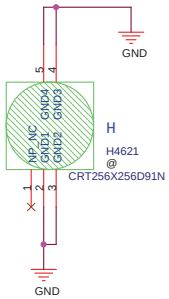


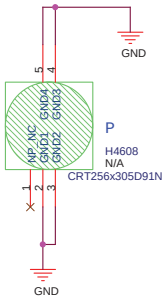


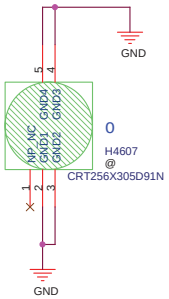


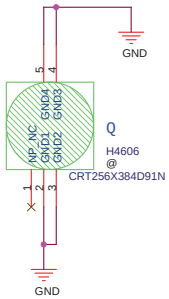


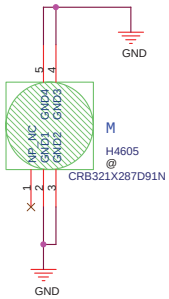


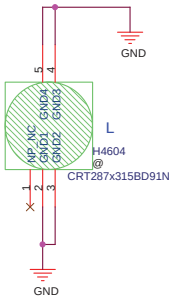


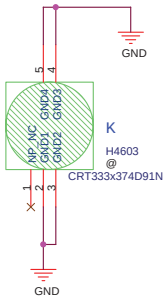


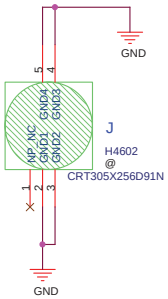


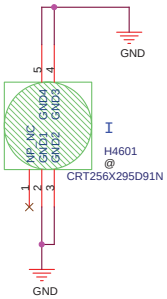


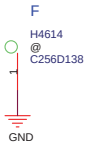


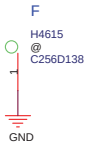


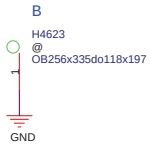


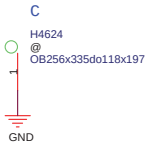


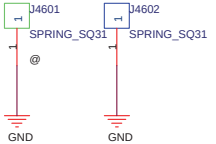












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<Variant Name>

ASUSTeK COMPUTER INC

Title : EMPTY

Engineer: Marco Chen

Size	Project Name	Rev
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R1.0 -> R1.1

1.Page 6: DNI R611 because Int. pull-up resister exists in FAN module.

2.Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

3.Page 17: Change reference name from F3602 to F1701.

4.Page 21: DNI U2103.

5.Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.

6.Page 23: Change R2301 size from 0603 to 0402.

7.Page 23: Add pull high resister R2306*DNI and pull down resister R2307*Mount for ODD cable select.

8.Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.

9.Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.Page 32: Delete R3201 and connect MIC2_VREFOUTto R3203.1 directly.

11.Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.

12.Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

13.Page 35: Change keyboard matrix.

14.Page 36: Change reference name from JP3403 to JP3601

15.Page 36: Change R3622 size from 0402 to 0603.

16.Page 39: Delete R3920 and change Q3906 and Q3907*2N7006 to Q3908*UM6K1N.

17.Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.

18.Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.

19.Page 34: Add ESD Protection*D3402 for Touch Pad.

20.Page 27: Add series resister 33 ohm for PCI_FRAME# and PCI_AD13

21.Page 34:Change Q3403**UM6K1N to Q3404, Q3405*2N7002.

22.Page 18: Change L1801, L1802, and L1803 from bead to inductor.

23.Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

24.Page 6: Change R615 pull up from +3VS to +5VS_AUDIO.

25.Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.

26.Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.

27.Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.

28.Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.

29.Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.

30.Page 45:Add L4506 and L4507 for EMI requirement.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 48 of 63	

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<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
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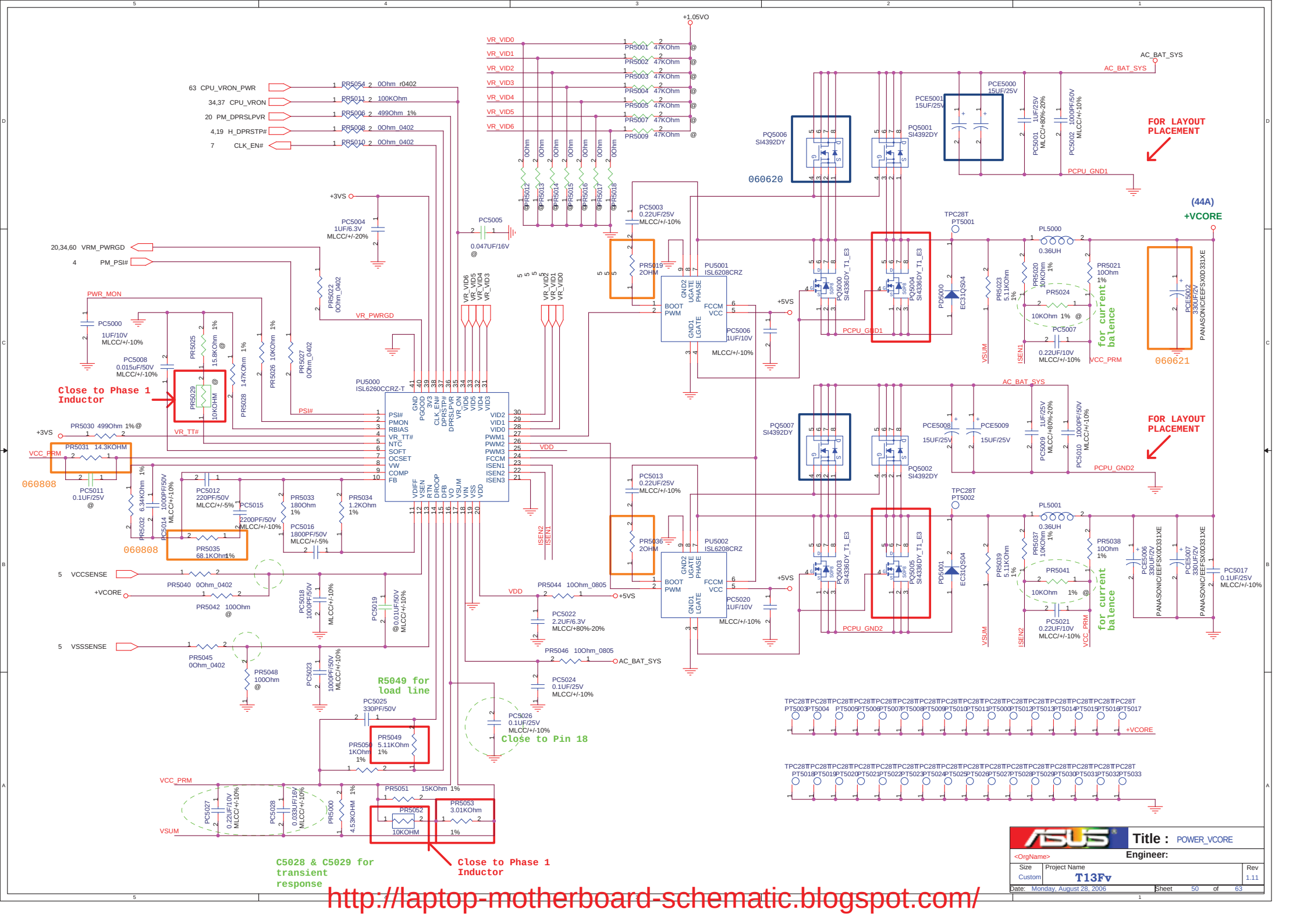

Title :	POWER_VCORE
<OrgName>	Engineer:
Size: Custom	Project Name: T13Fv
Rev:	1.11
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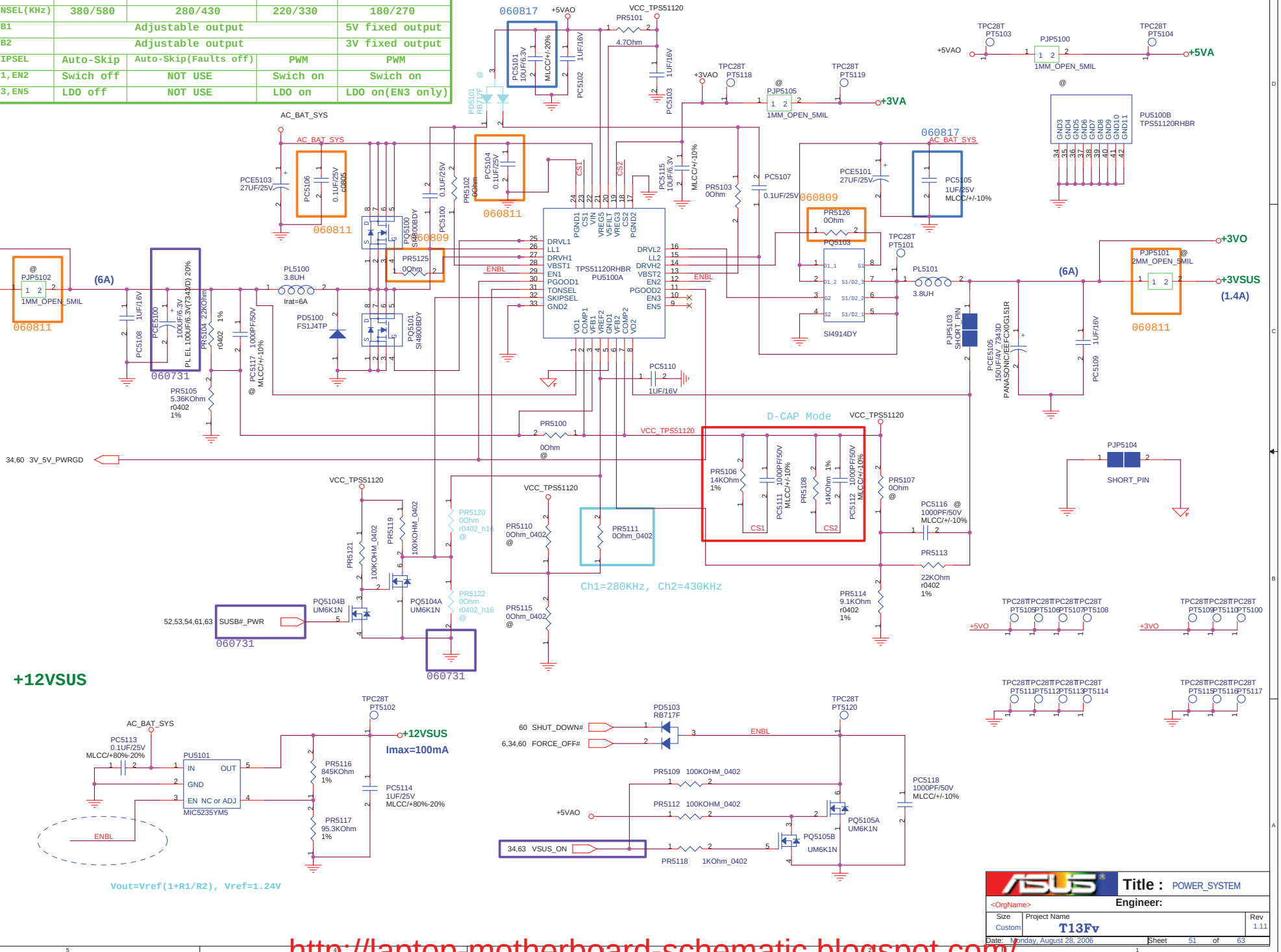
PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)



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Title :	POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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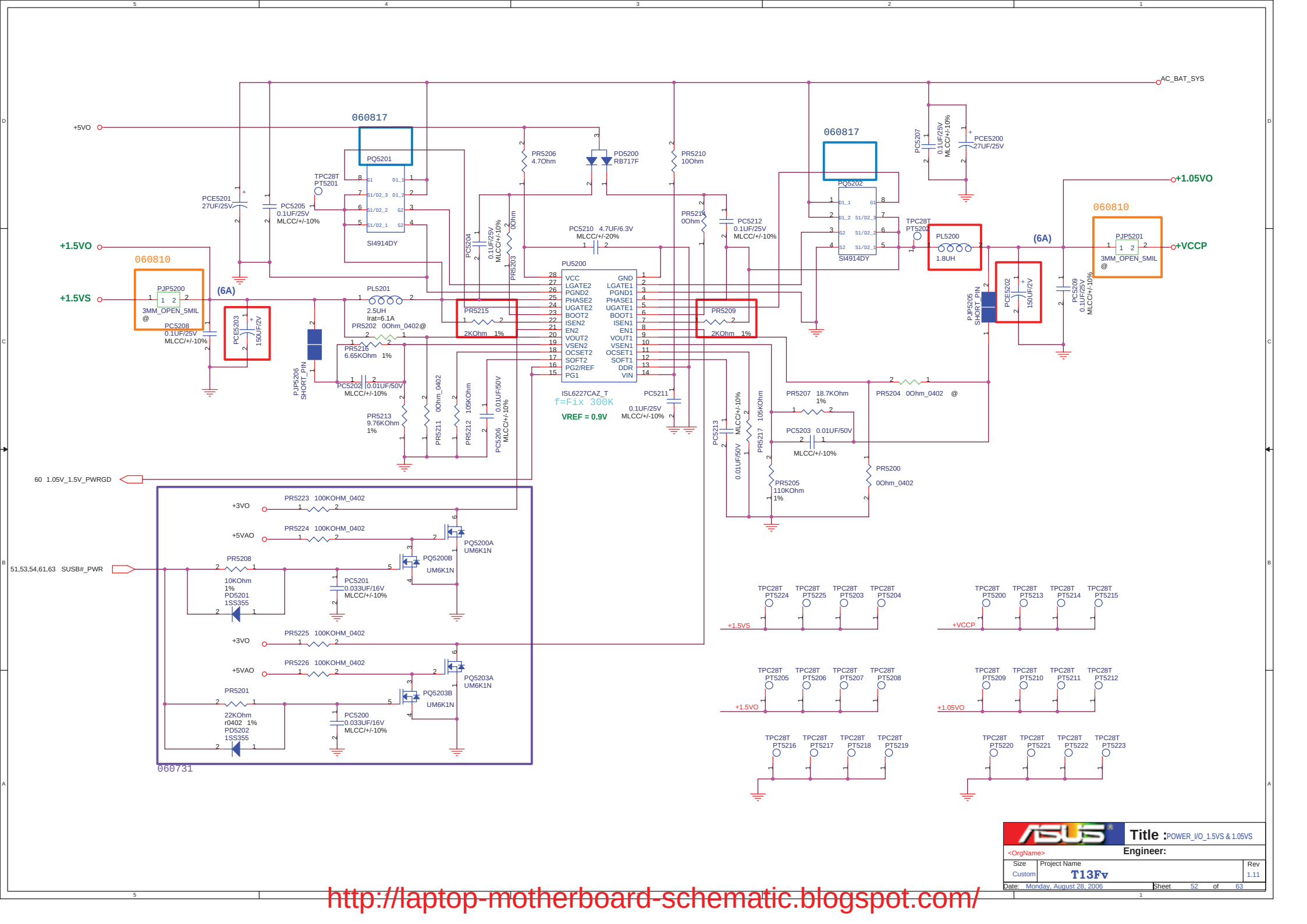
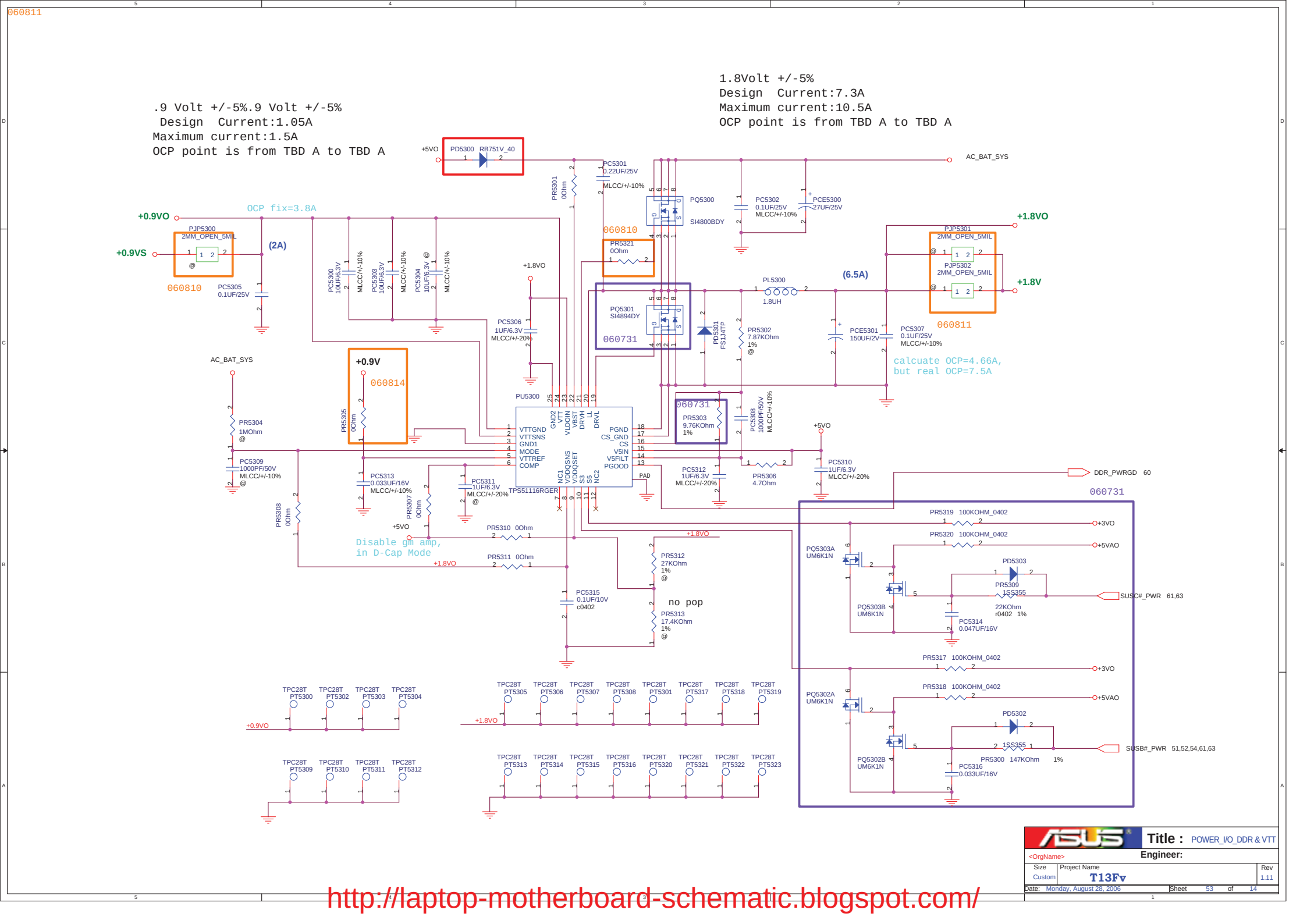


http://laptop-motherboard-schematic.blogspot.com/


060811
.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A
1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A
+5VO
PD5300 RB751V_40
AC_BAT_SYS
PR5301 0Ohm
PC5301 0.22UF/25V MLCC/+/-10%
PQ5300 SI4800BDY
PC5302 0.1UF/25V MLCC/+/-10%
PCE5300 27UF/25V
+0.9VO
OCP fix=3.8A
PJP5300 2MM_OPEN_5MIL
(2A)
+0.9VS
060810
PC5305 0.1UF/25V
PC5300 10UF/6.3V MLCC/+/-10%
PC5303 10UF/6.3V MLCC/+/-10%
PC5304 10UF/6.3V @ MLCC/+/-10%
+1.8VO
PR5321 0Ohm
PJP5301 2MM_OPEN_5MIL
PJP5302 2MM_OPEN_5MIL
+1.8V
060811
(6.5A)
PL5300 1.8UH
PQ5301 SI4894DY
060731
PD5301 FS1J4TP
PR5302 7.87KOhm 1%
PCE5301 150UF/2V
PC5307 0.1UF/25V MLCC/+/-10%
calcuate OCP=4.66A,
but real OCP=7.5A
PC5306 1UF/6.3V MLCC/+/-20%
AC_BAT_SYS
+0.9V
060814
PR5305 0Ohm
PR5304 1MOhm @
PC5309 1000PF/50V MLCC/+/-10% @
PU5300
VTTGND
VTTSNS
GND1
MODE
VTTREF
COMP
GND2
VTT
VLDOIN
VBST
DRVH
LL
DRVL
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
PAD
NC1
VDDQSNS
VDDQSET
S3
S5
NC2
TPS51116RGER
060731
PR5303 9.76KOhm 1%
PC5308 1000PF/50V MLCC/+/-10%
PC5310 1UF/6.3V MLCC/+/-20%
PC5312 1UF/6.3V MLCC/+/-20%
PR5306 4.7Ohm
DDR_PWRGD 60
PC5313 0.033UF/16V MLCC/+/-10%
PC5311 1UF/6.3V MLCC/+/-20% @
PR5307 0Ohm
PR5308 0Ohm
PR5310 0Ohm
PR5311 0Ohm
Disable gm amp,
in D-Cap Mode
PR5312 27KOhm 1% @
PC5315 0.1UF/10V c0402
no pop
PR5313 17.4KOhm 1% @
PR5319 100KOHM_0402
PR5320 100KOHM_0402
PQ5303A UM6K1N
PQ5303B UM6K1N
PD5303
PR5309 1SS355
22KOhm r0402 1%
PC5314 0.047UF/16V
SUSC#_PWR 61,63
PR5317 100KOHM_0402
PR5318 100KOHM_0402
PQ5302A UM6K1N
PQ5302B UM6K1N
PD5302
PR5300 147KOhm 1%
PC5316 0.033UF/16V
SUSB#_PWR 51,52,54,61,63
TPC28T PT5300
TPC28T PT5302
TPC28T PT5303
TPC28T PT5304
TPC28T PT5305
TPC28T PT5306
TPC28T PT5307
TPC28T PT5308
TPC28T PT5301
TPC28T PT5317
TPC28T PT5318
TPC28T PT5319
TPC28T PT5309
TPC28T PT5310
TPC28T PT5311
TPC28T PT5312
TPC28T PT5313
TPC28T PT5314
TPC28T PT5315
TPC28T PT5316
TPC28T PT5320
TPC28T PT5321
TPC28T PT5322
TPC28T PT5323
Title : POWER_I/O_DDR & VTT
<OrgName>
Engineer:
Size Custom
Project Name T13Fv
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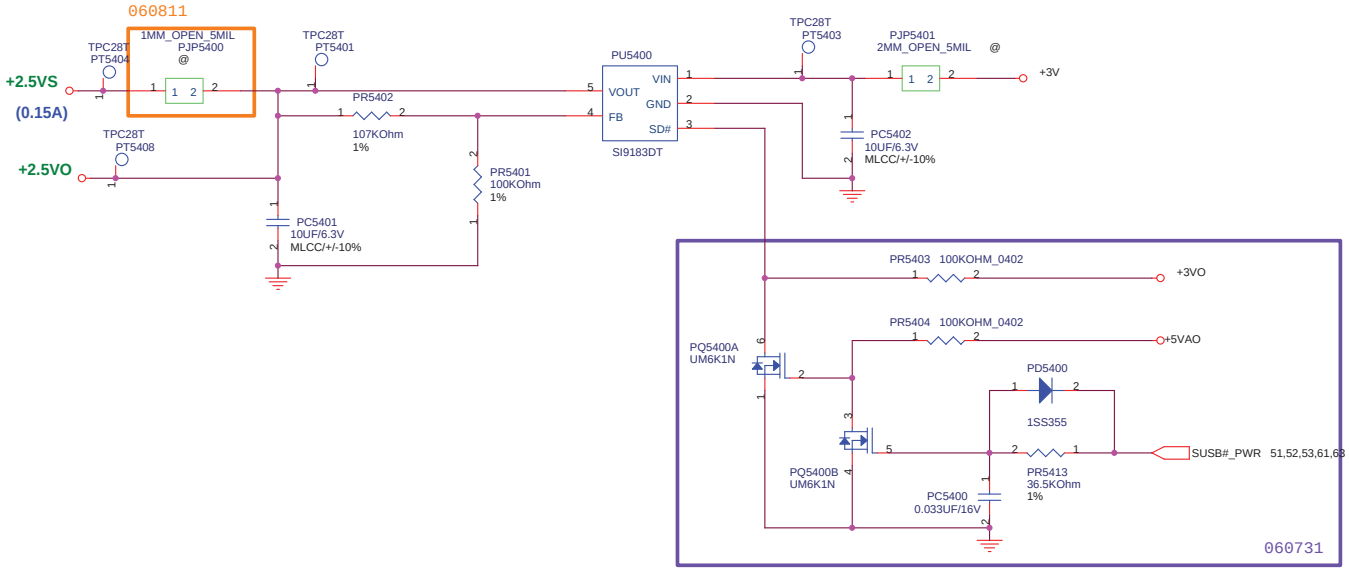
+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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Title : EMPTY

<OrgName>

Engineer:

Size	Project Name	Rev
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ASUS	Title : EMPTY			
<OrgName>	Engineer:			
Size: Custom	Project Name: T13Fv			Rev: 1.11
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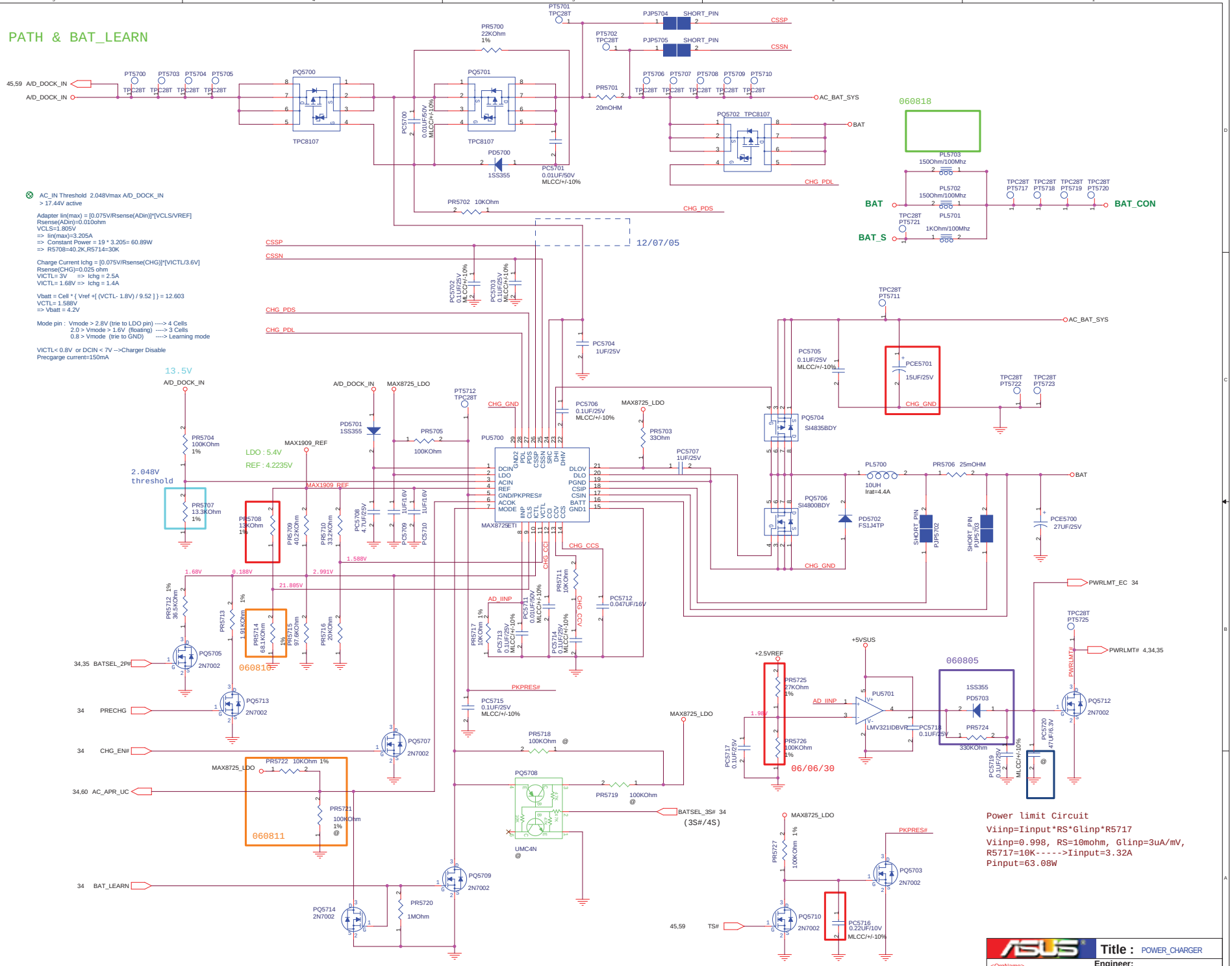
POWER PATH & BAT_LEARN



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Title : POWER_CHARGER		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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Title : POWER_PIC				
<OrgName>	Engineer:			
Size: Custom	Project Name: T13Fv			Rev: 1.11
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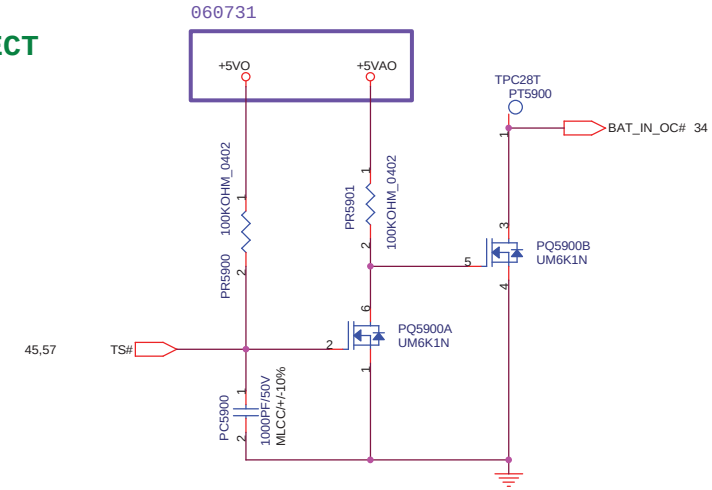
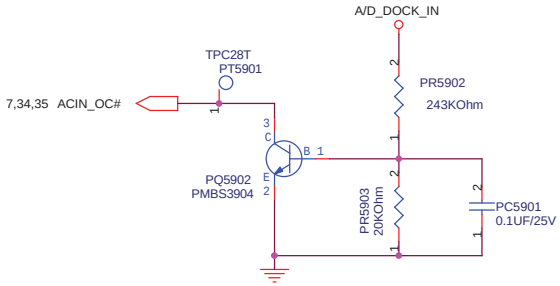
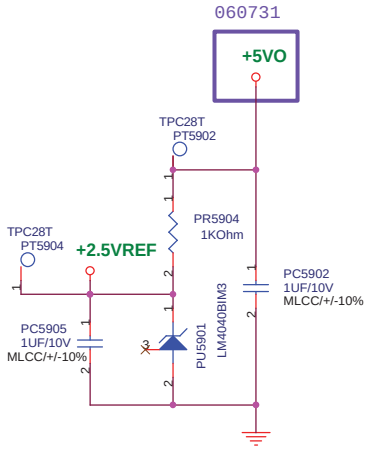
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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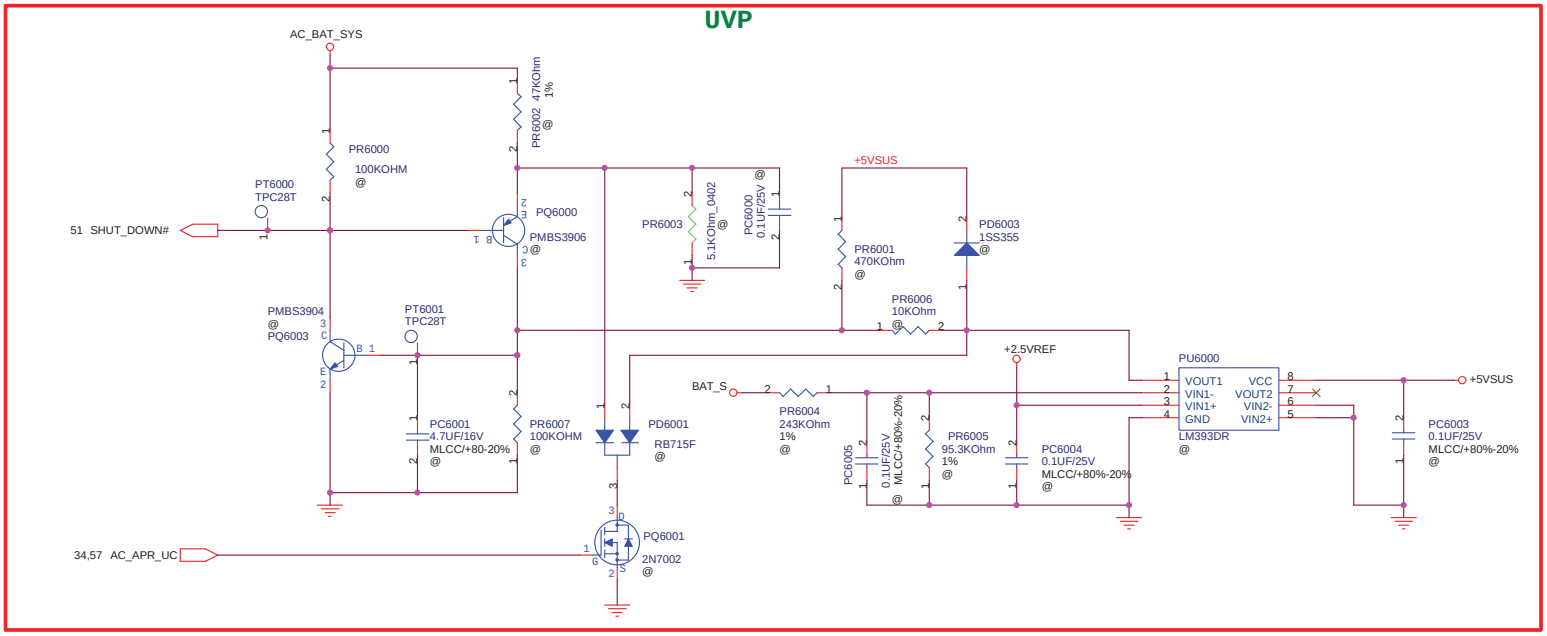
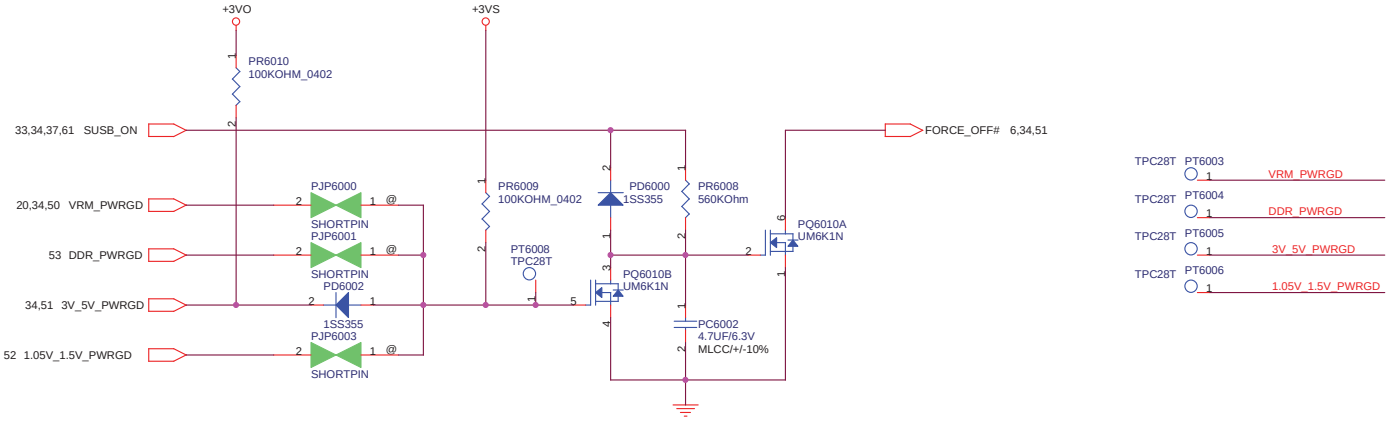
UVP



POWER GOOD DETECTER



Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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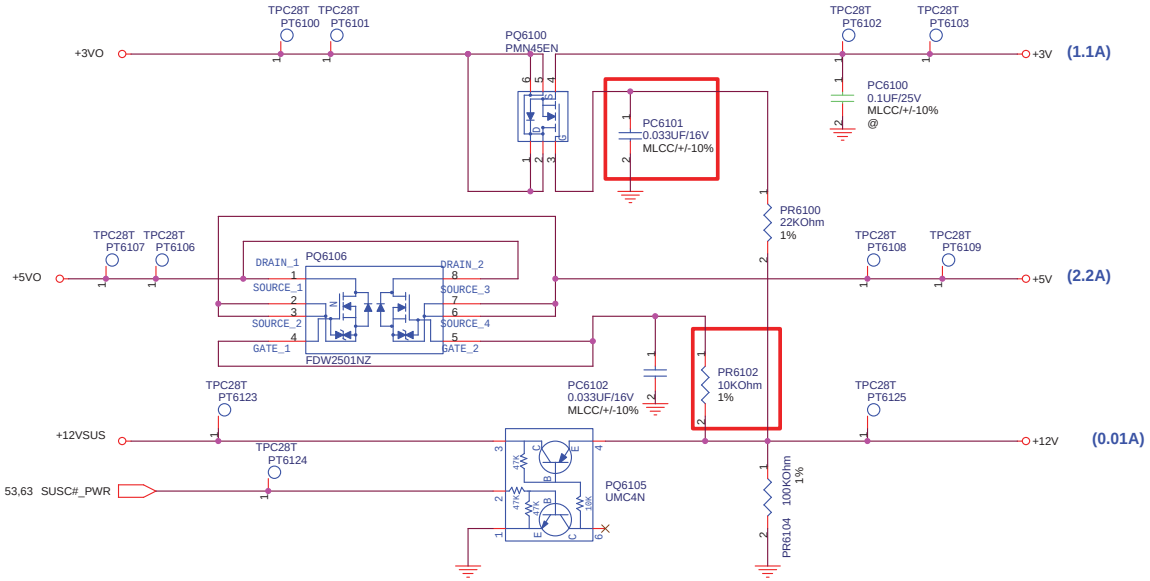
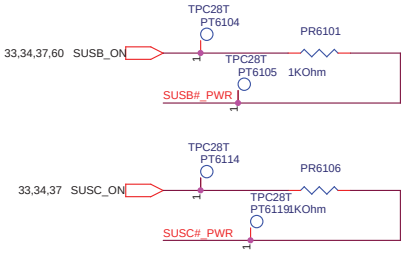
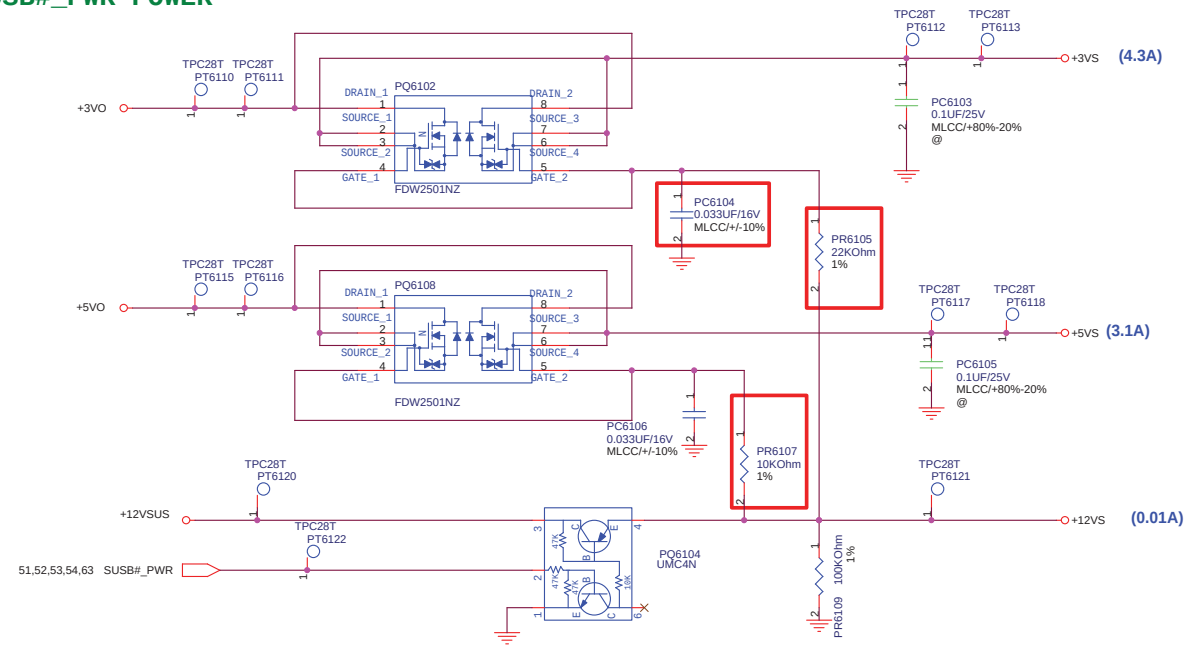
SUSC#_PWR POWER





SUSB#_PWR POWER



Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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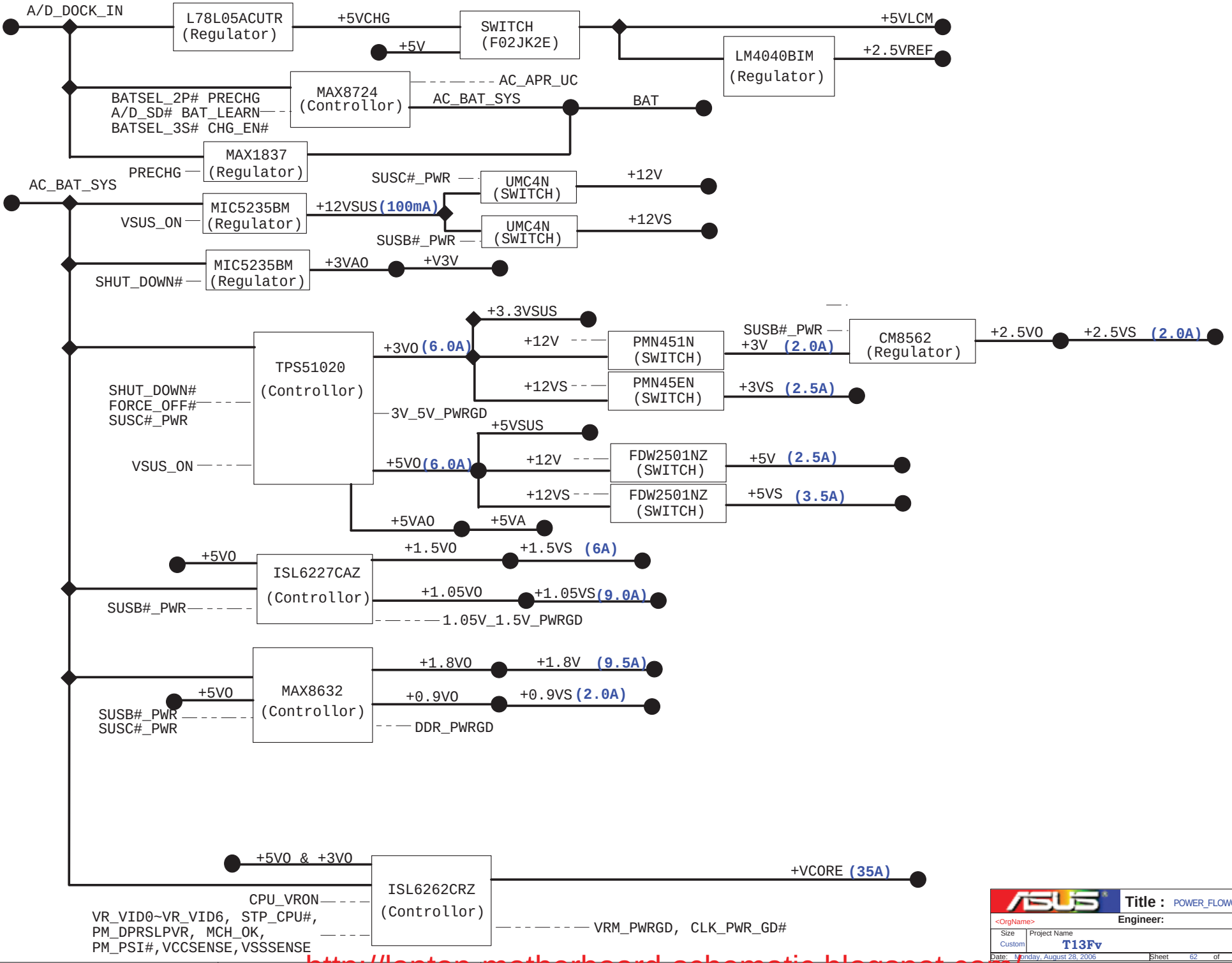

Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
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AC_BAT_SYS → AC_BAT_SYS 17,50,51,52,53,57,60

+3VA → +3VA 6,17,19,34,37,51

+5VA → +5VA 6,51

+5VO → +5VO 51,52,53,59,61

+3VO → +3VO 51,52,53,54,60,61

+3VSUS → +3VSUS 17,20,21,22,29,31,39,51

+5VSUS → +5VSUS 22,51,57,60

+3V → +3V 21,25,26,27,28,33,35,37,54,61

+3VS → +3VS 6,7,9,11,13,14,15,17,18,20,21,22,23,25,26,27,29,30,33,34,36,37,38,39,50,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 24,31,37,61

+12VS → +12VS 17,37,61

+5V → +5V 6,17,24,28,33,37,61

+5VS → +5VS 6,18,22,23,25,30,31,34,37,38,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 11,37,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 9,12,14,15,37,53

+VCCP → +VCCP 5,12,22,37,52

+0.9VS → +0.9VS 16,37,53

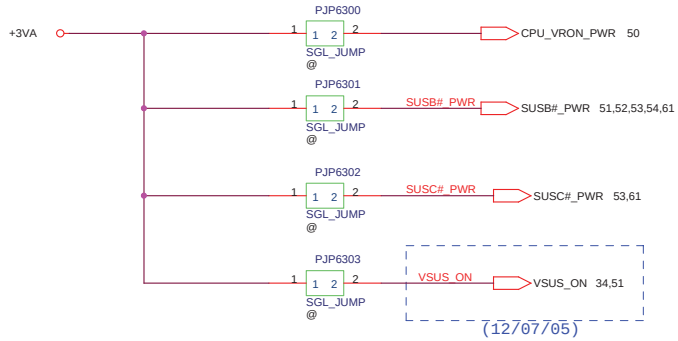
BAT → BAT 57

+2.5VREF → +2.5VREF 57,59,60

+VCORE → +VCORE 5,37,50

BAT_CON → BAT_CON 45,57

FOR POWER TEST



Title : POWER_SIGNAL			
<OrgName>	Engineer:		
Size: Custom	Project Name: T13Fv		Rev: 1.11
Date: Monday, August 28, 2006	Sheet 63 of 63		

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